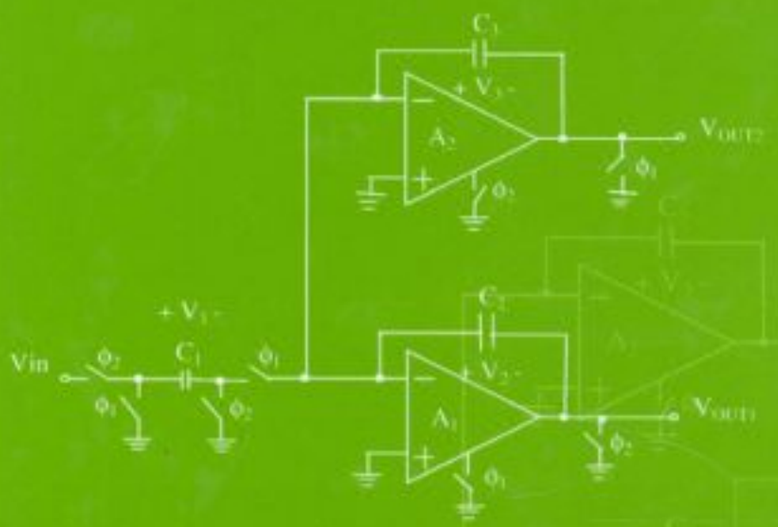
DESIGN OF LOW-VOLTAGE CMOS SWITCHED-OPAMP SWITCHED-CAPACITOR SYSTEMS

Vincent S.L. Cheung and
Howard C. Luong



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by

Vincent S.L. Cheung

Hong Kong University of Science & Technology

and

Howard C. Luong

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PREFACE

Voltage scaling in future sub-micron CMOS technology requires the gate-to-source (V_{GS}) voltage of transistor to operate in less than 0.9V by the year 2008 as predicted by the Semiconductor Industry Association. This has motivated new circuit techniques to be developed for low-voltage operation of analog circuits in recent years. In this research, the focus is on design and development of new switched-capacitor (SC) architectures and novel circuit techniques to implement high-performance SC systems to operate at low supply voltages. Emphasis is put on the design and development of the switched-opamp technique, which enables SC systems to operate with a supply voltage as low as the threshold voltages of the transistors in a given process. Detailed theoretical analyses and design limitations of the original switched-opamp technique are discussed in details. Following is the presentation of a novel multi-phase switched-opamp technique, which greatly improves the original switched-opamp technique in terms of operation speed and design compatibility with conventional SC architectures.

To improve the performance of switched-opamp systems, several new system architectures are proposed. A generic fast-settling double-sampling SC biquadratic filter architecture is proposed to achieve high-speed operation for SC circuits. Besides, a low-voltage double-sampling (DS) finite-gain-compensation (FGC) technique is employed to realize high-resolution $\Sigma\Delta$ modulator using only low-DC-gain opamps to maximize the speed and to reduce power dissipation. Furthermore, a family of novel power-efficient SC filters and $\Sigma\Delta$ modulators are built based on using only half-delay SC integrators. Lastly, single-opamp-based SC systems are designed for ultra-low-power applications. On the circuit level, a fast-switching methodology is proposed for the design of the switchable opamps for switched-opamp circuits to achieve switching frequency up to 50 MHz at 1 V, which is improved by about ten times compared to the prior arts.

The proposed multi-phase switched-opamp technique is verified with experimental results through the demonstration of a low-voltage SC pseudo-2-path filter implemented in a 0.5-μm CMOS process (V_{TP} = -0.85 V and

V_{TN} = 0.7 V). To demonstrate potential applications of the proposed multi-phase switched-opamp technique, additional four integrated circuits and systems have been designed and implemented in a standard 0.35-μm CMOS process (V_{TP} = -0.8 V and V_{TN} = 0.6V) to meet with different design corners such as the highest possible speed, the highest integration level, the highest power efficiency and the lowest possible power dissipation. A 10.7-MHz switched-opamp bandpass ΣΔ modulator is designed to operate at 1 V with the operation speed improved about 10 times compared to the existing designs at 1 V and comparable to other SC circuits operate at much higher supply voltages. A 1-V 3.5-mW switched-opamp quadrature IF circuitry demonstrates a practical design of a low-voltage, low-power and highly integrated SC system for Bluetooth receivers. In addition, designs of a 0.9-V single-switched-opamp-based ΣΔ modulator and a 0.9-V single-switched-opamp-based SC signal conditioning systems for pacemaker applications successfully illustrate the possibility to further reduce the power consumption to the sub-μW range.

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Vincent Sin-Luen Cheung
Howard Cam Luong
February 2003

Chapter 1

INTRODUCTION

1.1 Situation of Research

The trend towards low-voltage low-power single-chip systems has been growing quickly due to the increasing demand of smaller size and longer battery life for portable applications in all market segments including telecommunications, computers and consumer electronics. Meanwhile, single-chip implementation of both analog and digital systems in standard CMOS technology is recommended for lower cost, superior performance and smaller size. However, single-chip systems are not only difficult to design and implement but also face a new critical constraint imposed by voltage scaling in the sub-micron CMOS technology in recent years. Sub-micron CMOS technology shrinks the transistor size to boost for higher speed and lower power consumption, but it imposes reliability problems to the transistors at high voltage operation. As predicted by the Semiconductor Industry Association [SIA 99], MOS transistors are required to operate in less than 1.2 V by 2004 and 0.9 V by 2008, while their threshold voltages are kept more or less unchanged ($V_T \approx 0.7$ V ~ 0.9 V) to avoid excessive leakage current. At low-voltage operation (as low as 1 V), digital circuits can still attain reasonable performance, but most of the analog circuits even do not function. Nowadays, most analog circuits still need a supply voltage of at least 2 – 3 V for acceptable performance. As a result, low-power and low-voltage analog circuits solutions become essential to the development of single-chip systems in the near future.

Switched-Capacitor (SC) circuits [GRE 86, ANA 95] achieve high precision and low distortion. The performance of SC circuits depends mainly on capacitor matching that can be controlled very well (less than 0.1% error is possible with good layout technique), the circuit performance is therefore insensitive to process variation. On the other hand, the distortion in SC circuits is mainly determined by the linearity of its capacitor [CAS 95, STE 97] when the amplification of the opamp is high enough. As a result, the

quality of SC circuits is fairly independent to the reduction of the power supply. Nowadays, high dynamic range of between 50 dB to 80 dB can be achieved in SC circuits [DES 01, PEL 98a], even running at a supply voltage of less than 1 V. This is in contrast to the continuous-time designs, e.g. Gm-C designs [LIN 99], where the linearity of the opamp's is highly dependent on the available power supply voltage and where the distortion increases much more rapidly when the power supply voltage is decreased to very low voltages [CAS 95].

As a result, SC circuits generally achieve good and robust low-voltage performance than continuous-time circuits, and most of the recently reported 1-V CMOS filters [BAS97a, CHE 01] and ΣΔ modulators [BAS 97b, CHE 02b, PEL 98b] are implemented with SC circuits. Besides, some research works have been demonstrated to operate SC filters [BAS 00, CAS 90b] and ΣΔ modulators [GER 00a, CHE 02a] in the μ-W range while running at low supply voltages, which are both the key factors for most biomedical applications [SAN 96, STO 89]. Yet, at low-voltage operation, the operation speed of SC circuits drops dramatically. Figure 1.1 plots the operation frequency (sampling frequency) of some of the state-of-the-art SC circuits against the supply voltages.

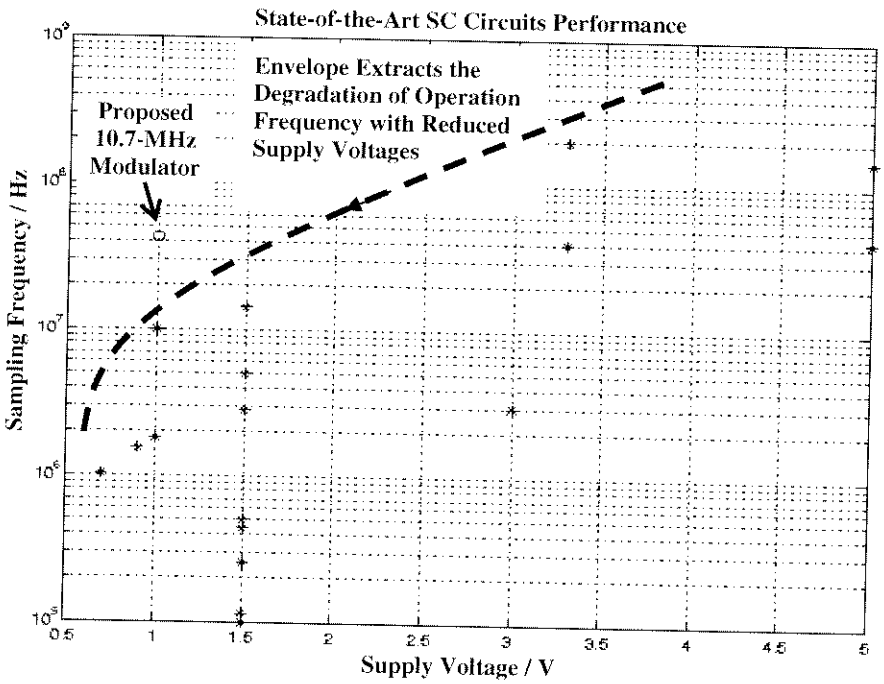


Figure 1.1 Plot of Operation Frequency (Sampling Frequency) of State-of-the-Art SC Circuits Against the Supply Voltages

The state-of-the-art performance of SC circuits operating at high supply voltages (~3 V to 5 V) can reach up to the hundred-MHz range, which makes them very attractive and useful for audio [ZWA 96, 97], video [BIR 98, GAL 96] and wireless communication applications [GUO 01, JAN 97]. Unfortunately, though both the precision and distortion are fairly independent to the supply voltage reduction, the operation frequency of SC circuits decreases in log-scale with the reduced supply voltages. At 1-V operation, prior arts demonstrated experimentally an operation speed of up to about 5 to 10 MHz, which is far lower than the attainable performance of SC circuits at higher supply voltages.

On the other hand, the power consumption of a SC circuit is quite linearly related to its operation frequency (sampling frequency) as shown in Fig. 1.2, which plots the power consumption (normalized to the number of poles of the system) of some of the state-of-the-art SC circuits against the operation frequency. Nevertheless, the power consumption of conventional SC circuits is fundamentally limited in the μ-W range by the efficiency of the architecture for systems and by the noise and leakage current considerations for circuits.

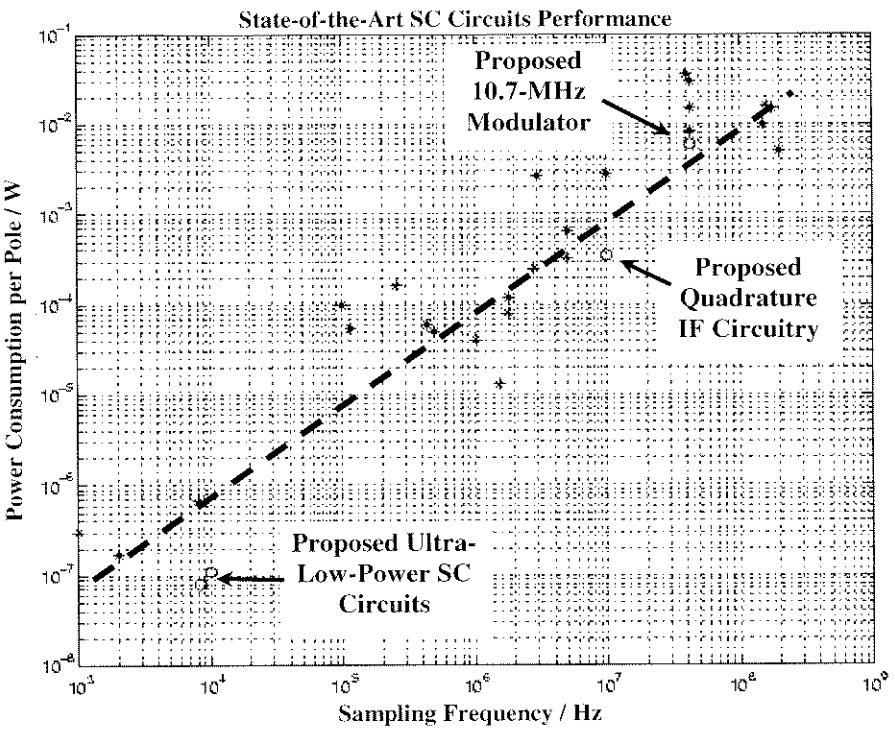


Figure 1.2 Plot of Power Consumption Per Pole Against Operation Frequency (Sampling Frequency) of the State-of-the-Art SC Circuits

1.2 Research Objectives

In this book, the objective is on the design and development of SC systems and circuit techniques to operate SC circuits at a supply voltage as low as 1-V. Special attention is paid on the switched-opamp (SO) technique [CRO 94, PEL 96, CHE 02b], which demonstrates very good and robust performance at low-voltage operation. Substantial emphasis is put on the development of high-speed and power-efficient switched-capacitor architectures to push the operation speed while reducing the power consumption. Four circuit prototypes are fabricated:

A circuit prototype for a 10.7-MHz SC bandpass ΣΔ modulator is realized to achieve a sampling frequency of up to 50 MHz, which is improved about five times compared to prior switched-opamp designs at 1-V operation as indicated in Fig. 1.1. A highly-integrated design of a 1-V switched-opamp IF circuitry for Bluetooth receiver is implemented. The quadrature channel consists of filters and ΣΔ modulator consumes a very low power consumption of only 350 μW per complex-pole pair. Lastly, sub-μW operation of a SC ΣΔ modulator and a SC signal-conditioning system are demonstrated at a 0.9-V supply. The circuit prototypes are realized using the developed power-efficient SC architectures to achieve for significant power reduction as can be observed in Fig. 1.2.

1.3 Outline of this Book

Chapter 2 discusses the primary challenges of designing SC circuits at low voltages. Problems of designing operational amplifiers (opamps) at low supply voltages and providing enough overdrive to turn on the MOS switches under low-gate-voltage operation are addressed. Four different approaches to solve the switch-driving problem are discussed: multi-threshold processes with low-threshold devices, voltage multiplication circuits, the local-bootstrapping technique and the switched-opamp techniques. The switched-opamp techniques are described in great details. Detailed analysis and comparison of the switched-opamp integrators with the conventional switched-capacitor integrators conclude to employ half-delay non-inverting SC integrator as the basic building block for realizing SC systems.

Chapter 3 presents the proposed high-speed and power-efficient SC architectures. This chapter begins with a brief review of the double-sampling technique. The limitations, in terms of compatibility and settling problems, of applying double-sampling technique on conventional SC architecture are addressed. A novel fast-settling double-sampling SC biquadratic filter is then proposed. On the other hand, based on the analysis of the switched-opamp

integrators in Chapter 2, switched-opamp technique is proven to be most power efficient to realize half-delay-SC-integrator while maintaining low sensitivity to the finite-opamp-gain effects as for the conventional SC integrators. A family of half-delay-SC-integrated-based filters and ΣΔ modulator are derived.

Chapter 4 discusses the circuit design of switchable opamp and layout issues for switched-opamp circuits. The fundamental limitations of the switching time of the conventional switchable opamp are addressed. Solutions to reduce the turn-on time of the switchable opamp for high-speed switched-opamp circuits are presented. Some layout considerations are discussed.

Chapter 5 presents the first circuit prototype that employs the proposed multi-phase switched-opamp technique to realize a low-voltage SC pseudo-2-path filter, which is not feasible to be constructed using the original switched-opamp technique. The application of the multi-phase switched-opamp on multi-phase SC systems is demonstrated through the realization of a low-voltage RAM-type SC pseudo-2-path integrator. The design considerations of using multi-phase switched-opamp technique are presented.

Chapter 6 describes a high-speed switched-opamp technique to implement a 1-V 10.7-MHz switched-opamp bandpass ΣΔ modulator for wireless applications. The chip prototype demonstrates a sampling frequency of up to 50 MHz, which is improved about five times compared to prior switched-opamp designs and comparable to the performance of the state-of-the-art SC circuits that operate at much higher supply voltages. A low-voltage finite-gain-compensation (FGC) technique that significantly reduces the DC gain requirement of opamps is presented and applied into the proposed fast-settling SC biquadratic architecture to realize the ΣΔ modulator. Low-voltage circuit building blocks are described from which a novel fast-switching current-mirror opamp is proposed. The measurement results of the ΣΔ modulator are presented.

Chapter 7 presents a high-level integration of switched-opamp filters and ΣΔ modulator to realize a 1-V CMOS quadrature IF circuitry for a wireless receiver for Bluetooth applications. To operate at a single 1-V supply, switched-opamp technique is employed to realize the half-delay-SC-integrator-based biquadratic filter, ladder filter and ΣΔ modulator topologies for the quadrature IF circuitry. As described in Chapter 3, half-delay-SC-integrators-based architectures require the opamp to be active only during the integration phase, which allow up to 50 % power reduction to the whole system and lead to a low power consumption of 350 μW per complex pole for the quadrature IF circuitry. The issues on time-sharing the active elements among the quadrature channels to enjoy both better channel matching and lower power consumption are discussed.

Chapter 8 describes design considerations to further reduce the power consumption to the sub-μW range while achieving robust operation at low supply voltages using switched-opamp technique. Two single-switched-opamp-based designs for pacemaker applications are presented. Design issues on time multiplexing of a single opamp to realize a high-order switched-capacitor system are addressed. By employing a multi-phase switched-opamp technique and one switchable opamp, sub-μW operation of a ΣΔ modulator and a switched-capacitor signal conditioning system are demonstrated at a single 0.9-V supply. Robust operation is also observed for both designs at supply voltages from 0.8 V to 1.2 V.

Chapter 9 gives the final conclusion with a summary of the potential applications for the proposed system architectures and design techniques.

Appendices provide reviews on basic analytical skills and design methodologies for switched-capacitor circuits.

Chapter 2

ANALYSIS AND DESIGN CONSIDERATIONS OF SWITCHED-OPAMP TECHNIQUES

2.1 Introduction

SC circuits consist of three types of components: capacitors, operational amplifiers (Opamp) and MOS switches. A standard CMOS process with either double-poly or linear-capacitor options provides linear integrated capacitors, which do not have any voltage supply requirements for proper operation. Though transistor stacking should be avoided in designing the opamps for maximum output swings at low-voltage operation, multi-stage operational amplifier [CHE 00a, FAN 97] (Opamp) topologies could still, in general, be designed at a very low supply voltage (sub-1-V operation is still possible) while achieving sufficient gain and bandwidth for SC circuits. The switches' driving capability, however, becomes the main limitation for supply voltages reduction. The minimum supply voltage required by most SC circuits is primarily determined and limited by the turn-on requirement of the switches that have to be able to switch the total signal swing. Usually this occurs for switches that are connected to the output of opamps. In this chapter, the existing solutions for improving the switches driving capabilities are briefly discussed. Then the principle of the Switched-Opamp (SO) technique [CRA 95, CRO 94] is introduced. After that, a few key modifications of SO techniques are described. Comparisons, in terms of opamp-gain sensitivity and power efficiency, between switched-opamp and switched-capacitor are carried out based on the realizations of two conventional parasitic-insensitive integrators. The comparison results suggest using half-delay switched-capacitor integrator as the basic element to implement any kind of switched-opamp architectures to save 50% power consumption while maintaining the same or even less opamp-gain sensitivity as the SC implementations.

2.2 Minimum Supply Voltage for SC Circuits

Figure 2.1 illustrates a SC integrator operating at a 1-V supply. Complementary switches are employed at the output of the opamp for maximal output swing. A two-stage opamp topology [GRA 93] is chosen as an example here because it delivers the maximum output swing while providing high DC gain even running under a very low supply voltage.

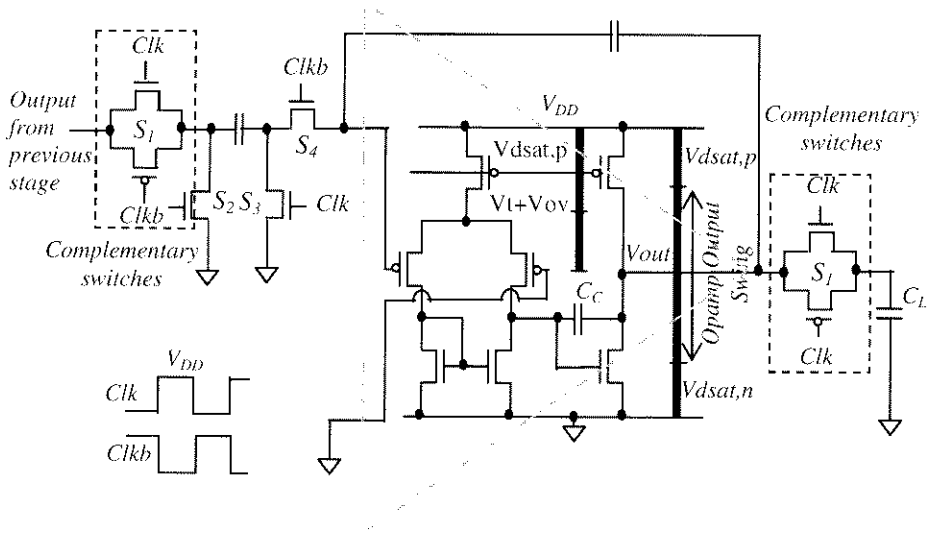


Figure 2.1 Schematic of a Two-Stage Opamp with a Pair of Complementary Switches Connected at the Output

Proper operation of this two-stage opamp requires careful biasing of the DC operating points of its input and output terminals. At a 1-V supply, the opamp can operate at high performance by setting the DC operating points of the input and output terminals at ground and 0.5V respectively. By setting the output DC point at the middle of the rails, an output swing of 0.7V (0.15V to 0.85V) can easily be achieved. Such an output swing is usually sufficient for most of the applications. However, when taking into consideration the operation swing of the pair of complementary switches, there is no useful swing at all for SC circuits to operate at a 1-V supply. This is illustrated in Fig. 2.2, which plots the conductance of a properly scaled complementary switch (both NMOS and PMOS devices are scaled to have same on-resistance) against the output signal level of the opamp.

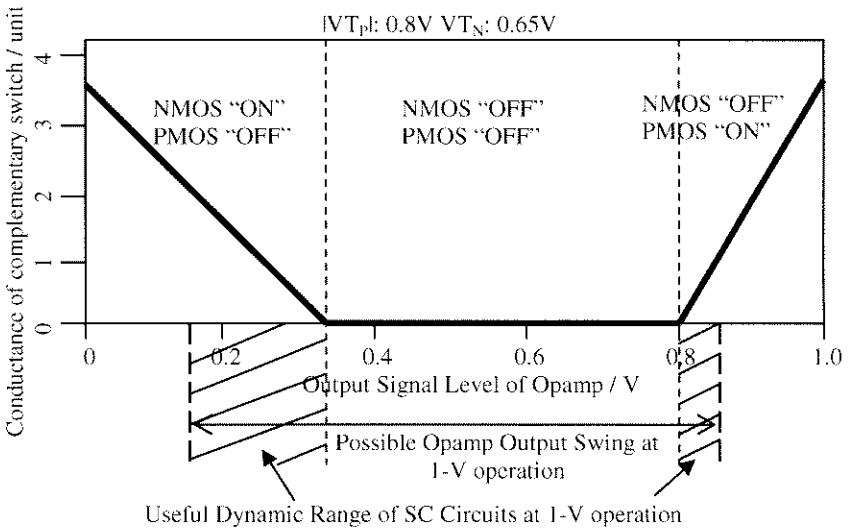


Figure 2.2 Plot of Conductance of a Pair of Complementary Switch

Implemented in a standard CMOS process (VT_N=0.65V, $|VT_P|$=0.8V) and a 1-V supply, there exists region where the pair of complementary switches is completely turned off. More seriously, this dead-zone region overlaps with most of the opamp signal swing. As indicated in Fig. 2.2, the usable output range is now only between 0.15 V to 0.35 V and 0.8 V to 0.85 V in this example. As a result, the actual useful output swing of an opamp used in a 1-V SC circuit is dramatically reduced to a level that is not useful at all for any application. Lastly, it is worth to point out that the rest of the NMOS switches (S_2, S_3 and S_4) can be referenced to a constant voltage (connected to the ground in this illustration), which makes it possible to operate these switches with enough driving voltages even at a 1-V supply.

2.3 Low-Voltage Solutions for SC Circuits

Existing solutions of low-voltage operation of SC circuits include using low-V_T devices [BAZ 95], on-chip voltage multiplier [CAS 90a, NIC 96], local switch bootstrapping technique [DES 01, COB 00] and switched-opamp (SO) techniques [CRO 94, PEL 98a, CHE 01, KES 01]. The first solution is to employ MOS switches with low threshold voltages (0.1V ~ 0.2V) so as to improve the driving capability of the switches under low-voltage operation. Unfortunately, in addition to the increased leakage and distortion problem, the cost of using this kind of special process is usually too high to be attractive.

The second solution employs on-chip voltage multiplier [CAS 90a, NIC 96] to boost the clock signals to drive the MOS switches while operating opamps at low-voltage. However, the voltage multiplier generates a lot of noise and dissipates a large portion of power of the whole circuit. More importantly, the employed technology must be able to withstand the generated high voltages from the voltage multiplier. As predicted by the Semiconductor Industry Association [SIA 99], voltage scaling in future submicron CMOS technology would require all transistors' gate-to-source (V_{GS}) voltages to operate in less than 0.9 V by the year 2008. As a result, this technique can no longer be used in the future submicron CMOS technology due to voltage scaling.

Local switch bootstrapping technique [ABO 99, DES 01] employs charged capacitor to keep the gate-to-source voltage (V_{GS}) of MOS switches equal to V_{DD}. The operation makes the on-resistance of the MOS switches independent of the input signal level and so low-voltage operation is possible. The main concern of the local switch bootstrapping technique is, however, still on the reliability issue of the devices. It is because this technique needs to bias the gate-to-body voltage of the device to be higher than the supply voltage.

2.4 Original Switched-Opamp Technique

Switched-opamp (SO) technique [STE 93, BAS 94, CRO 94] has been shown to be a promising low-cost solution to realize SC circuits in standard CMOS processes. The SO technique basically eliminates those critical MOS

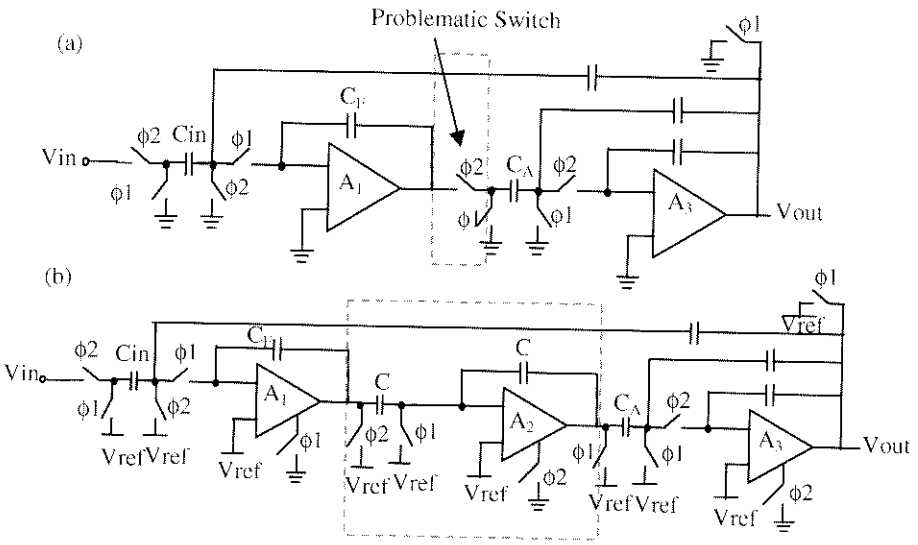


Figure 2.3 Simplified Topology of a SC Biquadratic Filter
(a) Classical Switched-Capacitor Version, (b) Switched-Opamp Version

switches that set the minimum supply voltage to allow sub-1-V operation of SC circuits without reliability problem. The original SO technique can be explained by considering a classical SC biquadratic filter and its corresponding SO version as shown in Fig. 2.3.

As explained in section 2.2, the MOS switch (problematic switch) that connects at the output of opamp A_1 has to drive the full signal swing and thus limiting the minimum supply voltage that can be used for operating SC filters. The switched-opamp technique [CRO 94] employs a unity-inverting delay SC integrator to replace the problematic switch that connects at the output of opamp A_1, as indicated in the dotted blocks in Fig. 2.3. As a result, there only remain MOS switches that are either connected directly or virtually to a reference voltage (V_{REF}). With the use of dynamic level shifters [BAS 97a, CHE 00b, PEL 98b], the common-mode input voltage and the quiescent output voltage of the opamp can be set independently such that the reference voltage (V_{REF}) can be set either at ground or V_{DD}. Hence, even operating at a 1-V supply, those remaining MOS switches that connect either directly or virtually to the reference voltage will be provided sufficient driving voltages. On the other hand, the operation of the switched-opamp technique requires to turn-off all opamps after their integration phase. This is to preserve the

Table 2.1 Performance Summary of Low-Voltage SC Circuits Using Original SO Technique

Design	[CRO 94]	[BAS 97a]	[PEL 97a]	[M.KES 01]	[SAU 02]
Technique	Switched-Opamp				
Technology	2.4-μm CMOS	0.5-μm CMOS	0.5-μm CMOS	0.35-μm CMOS	0.5-μm CMOS
Voltage	1.5 V	1.0 V	0.9 V	1.0 V	0.7 V
Threshold Voltages	VT_N: 0.9V $\lvert VT_P\rvert$: 0.9V	VT_N: 0.65V $\lvert VT_P\rvert$: 0.7V	VT_N: 0.62V $\lvert VT_P\rvert$: 0.55V	VT_N: 0.55V $\lvert VT_P\rvert$: 0.55V	VT_N: 0.43V $\lvert VT_P\rvert$: 0.38V
Sampling Frequency	115 kHz	1.8 MHz	1.538 MHz	10.24 MHz	1.024 MHz
Center Frequency	NA	435 kHz	NA	NA	NA
Bandwidth	1.5 kHz	65 kHz	16 kHz	50 kHz	8 kHz
Order	Second	Second	Third	Second	Second
Type	Lowpass Filter	Bandpass Filter	Lowpass ΣΔ Modulator	Lowpass ΣΔ Modulator	Lowpass ΣΔ Modulator
Peak SNDR	NA	NA	62 dB	78 dB	79 dB
Dynamic Range	69 dB	52 dB	77 dB	74 dB	86 dB
Chip Area	1.14 mm^2	0.15 mm^2	0.85 mm^2	0.41 mm^2	0.082 mm^2
Power	110 μW	160 μW	40 μW	5.6 mW	80 μW

charge (interested signal) in the integration capacitors (e.g. C_F of A_1 in Fig. 2.3) and prevents static current from flowing into the opamp outputs, which are tied to a reference voltage (V_{REF}) after the integration phase. Implemented in a standard CMOS process, switched-opamp filters [CRO 94, BAS 97a], ΣΔ modulators [PEL 97a, J. SAU 02, KES 01] and pipeline analog-to-digital converters (ADC) [WAL 01] have been demonstrated successfully to operate in a supply voltage as low as 0.7 V in recent years. Table 2.1 summarizes the state-of-the-art performance of low-voltage SC circuits using the original switched-opamp technique.

It can be observed that switched-opamp circuits generally achieve very good performance at both low power consumption and supply voltages. Though the dynamic range of most analog circuits, such as Gm-C filters, would be reduced dramatically at low-voltage operation, switched-opamp circuits can still maintain a fairly high dynamic range of more than 45 dB (more than 7-bit resolution), which is sufficient for many nowadays applications. Yet, as can be observed from Table 2.1, switched-opamp circuits at 1-V operation can only achieve an experimentally reported operation speed up to about 10 MHz, which is in fact still far lower than the attainable performance of SC circuits at higher supply voltages. The operation speed has been improved by switching off only the output stage of a two-stage amplifier after the integration phase [BAS 97a, CHE 02b] while maintaining the input stage active at all time. The required turn-on time of the output stage of the opamp becomes one of the main limitation factors of switched-opamp circuits. In addition, since the original switched-opamp technique requires isolating the opamp from the signal path by turning off completely either the whole opamp or its output stages (for a two-stage amplifier approach) after the integration phase, these switched-opamp techniques cannot be employed to realize many useful SC circuits, such as SC pseudo-N-path filters [INO 86, PAL 89, FRA 96] and opamp-gain-compensation techniques [KI 91, NAG 97], which require the opamps to be active at all phases in the system for signal processing.

2.5 Multi-Phase Switched-Opamp Technique

A multi-phase switched-opamp technique [CHE 99] has been proposed to improve the performance of the SO techniques in terms of operation speed and compatibility with existing SC circuits. The multi-phase switched-opamp technique improves the compatibility of the original switched-opamp techniques on switched-capacitor circuits by employing the additional switchable opamp (A_1') that is put in parallel but operated in alternative phase with the original switchable opamp (A_1). Figure 2.4 shows a fully-differential universal integrator (though differential structure is shown,

single-ended version is also viable) that uses the modified switched-opamp technique for low-voltage switched-capacitor applications.

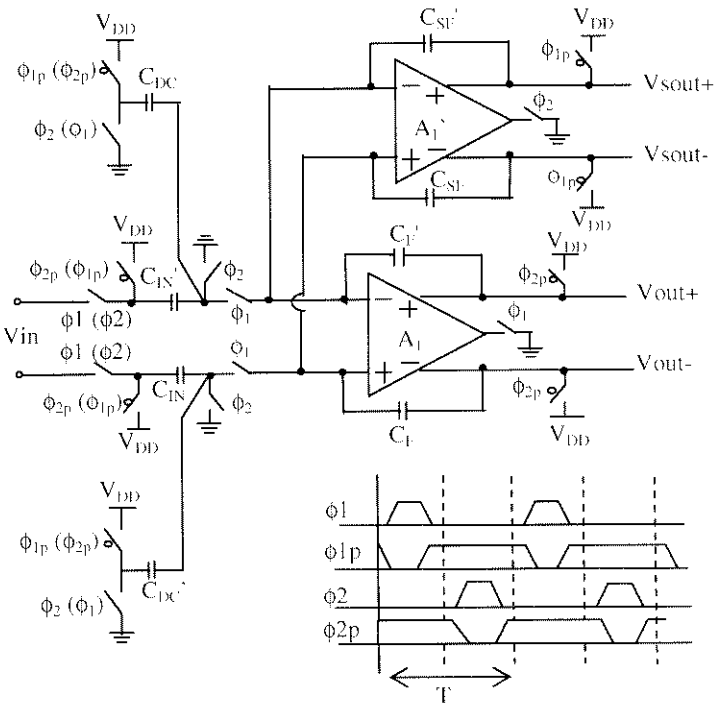


Figure 2.4 Low-Voltage Fully-Differential SC Integrator Using Multi-Phase Switched-Opamp Technique

$\phi_{1,2}$ and $\phi_{1p,2p}$ are complementary clock phases for NMOS and PMOS switches, respectively. The dynamic level shifters in [BAS 97a] are adopted and implemented with switching capacitors C_{DC} and C_{DC}', which are half as large as the input capacitors C_{IN} and C_{IN}' respectively. By so doing, the common-mode input voltage of two switchable opamps are biased at ground, while their outputs, in steady state without input signal, are biased to middle of rails by the use of common-mode feedback circuits. The two switchable opamps are turned on and off alternatively in two complementary non-overlapping clock phases. In ϕ_1, opamp A_1 is turned on to integrate the sampled signal from C_{IN} (C_{IN}') and the stored signal in C_{SF} (C_{SF}'), while the processed signal is stored in the integration capacitors C_F (C_F'), which is charged to V_{DD} in previous ϕ_2 cycle. In ϕ_2, opamp A_1' is turned on and the opamp A_1 is turned off with its outputs (V_{out+}, V_{out-}) shorted to V_{DD}. In this case, C_F (C_F') is charged to V_{DD} while the signal that stored in C_F (C_F') is passed to C_{SF} (C_{SF}'), which is charged to V_{DD} previously in ϕ_1. When ϕ_1 comes again, opamp A_1 is turned on, while opamp A_1' is turned off with its outputs shorted to V_{DD}. By doing so, the signal is passed back to C_F (C_F')

again while opamp A_1 is integrating with new sampled signal from C_{IN} (C_{IN}'). Equation 2.1 describes the situation mathematically.

$$\left.\begin{aligned} Vout^{+}(nT) &= \left(\frac{C_{SF}}{C_F}\frac{C_F}{C_{SF}}\right)Vout^{+}(nT-T) - \frac{C_{IN}}{C_F}Vin(nT)^{+} \\ Vout^{-}(nT) &= \left(\frac{C_{SF}}{C_F}\frac{C_F}{C_{SF}}\right)Vout^{-}(nT-T) - \frac{C_{IN}}{C_F}Vin(nT)^{-} \end{aligned}\right\} \quad \text{(Eq.2.1)}$$

It can be observed that capacitors C_{SF} and C_{SF}' in the Equation 2.1 are cancelled and hence even capacitors C_F and C_{SF} (as well as C_F' and C_{SF}') are not matched, the output signal obtained in previous cycle still reappears at the virtual ground of opamp A_1. The design is optimal when all capacitors C_F, C_F', C_{SF} and C_{SF}' have the same value. If the storage capacitors C_{SF} and C_{SF}' are smaller than the integrating capacitors C_F and C_F', the signal would be amplified by the ratio (C_{SF}/C_F or C_{SF}/C_F') when it is stored and thus more signal dynamic range would be required from the opamp to prevent it from being distorted. On the other hand, using storage capacitors that are larger than the integrating capacitors would slow down the speed of operation, and increase the chip area.

The multi-phase switched-opamp integrator can also be operated with a low supply voltage. Besides, with the addition of a switchable opamp A_1', the output signal is available for processing in both clock phases, as if a classical SC integrators. As a result, this multi-phase switched-opamp integrator can be directly applied to replace the classical SC integrators in any low-voltage SC applications. This would save a lot of re-designing efforts to implement SC circuits at low voltage because the modified switched-opamp technique can be directly adapted to nearly all of the existing SC synthesizing methods. More importantly, due to the creation of an idle phase in this switched-opamp integrator, useful techniques like pseudo-N-path [CHE 00b, CHE 01] and opamp-gain-compensation [CHE 02b, CHE 02b] can be implemented in a very low supply voltage in a standard CMOS technology.

The performance of the multi-phase switched-opamp technique can be further improved with a special design of the switchable opamp. The idea comes from the fact that in the multi-phase switched-opamp technique, the input terminals of the two switchable-opamps A_1 and A_1' in Fig. 2.4 are connected together, while only one of the two opamps is turned on at a time. As such, it is useful to share the input stage of the two switchable-opamps if a two-stage amplifier approach is adopted. This result in the design of a single two-stage amplifier with one differential input stage and two pairs of differential output stages that are turned on and off alternatively. As mentioned previously, the turn-on time of the switchable opamp can be

improved by maintaining the input stage of the opamp active at all time while only switching on and off of the output stages. To demonstrate the idea, a multi-phase switched-opamp integrator, which utilizes a fully-differential two-stage amplifier with dual-time-multiplexing-switchable-output-pair is shown in Fig. 2.5 below.

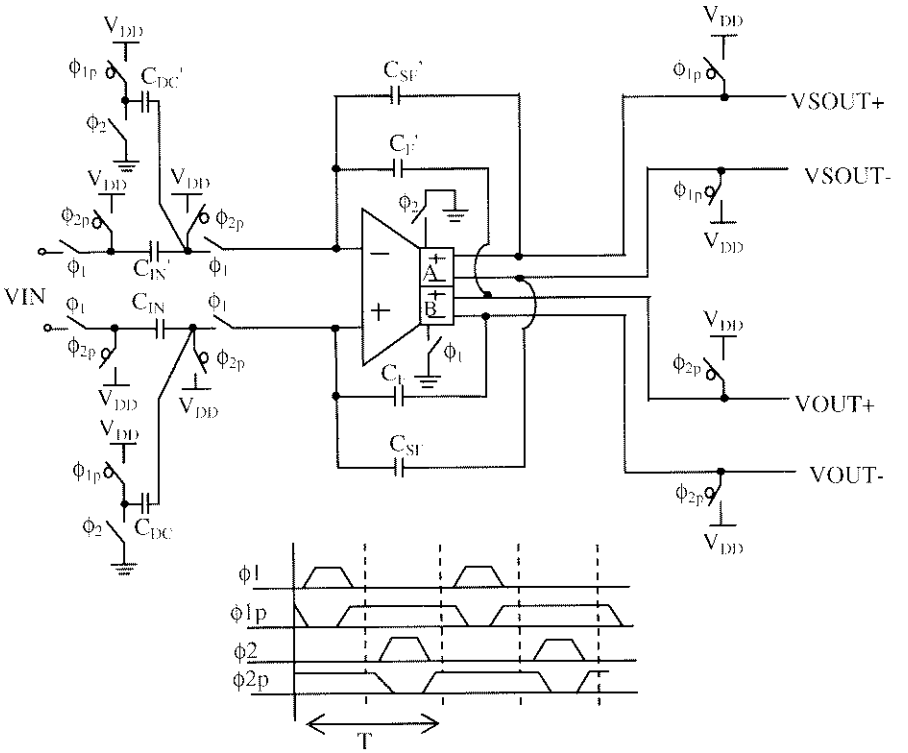


Figure 2.5 Optimized Switched-Opamp Integrator Using the a Fully-Differential Two-Stage Opamp with Dual-Time-Multiplexed-Output-Stages

Similarly, the optimized multi-phase switched-opamp integrator [CHE 00b] employs two identical capacitors C_F and C_{SF} (C_F' and C_{SF}') as the integrating capacitors. At ϕ_2, the output "B" of the switchable opamp is shorted to the supply (V_{DD}) after its integration phase ϕ_1, the signal stored in C_F (C_F') is passed to C_{SF} (C_{SF}') through the virtual ground of the opamp and the signal re-appears at the output "A" of the opamp. During ϕ_1, this stored signal in C_{SF} (C_{SF}') is re-injected into C_F (C_F') to integrate with a new input sample. As such, the output signal is available for processing at both clock phases though appears at different nodes. Since the input stage of the opamp is always maintained active, the optimized multi-phase switched-opamp technique can achieve higher operation speed than the original multi-phase

switched-opamp technique. On the other hand, as there is only one output stage turned on at a time, the optimized multi-phase switched-opamp integrator dissipates one unit of opamp power, which is same as a conventional SC integrator. As will be shown in this book, with the employment of the optimized multi-phase switched-opamp technique, further speed enhancement of switched-opamp circuits can be achieved with tailor-made designs of SC systems and switchable opamps.

2.6 Analysis of Parasitic-Insensitive Switched-Capacitor and Switched-Opamp Integrators

2.6.1 Analysis of Conventional Parasitic-Insensitive SC Integrators

Conventional switched-capacitor circuits [GRE 86] employ parasitic-insensitive SC integrators as the basic building blocks for realizing the required z-domain transfer functions such that the overall architecture also enjoys low parasitic sensitivity. Figure 2.6 shows the schematic of a parasitic-insensitive SC integrator [GRE 86].

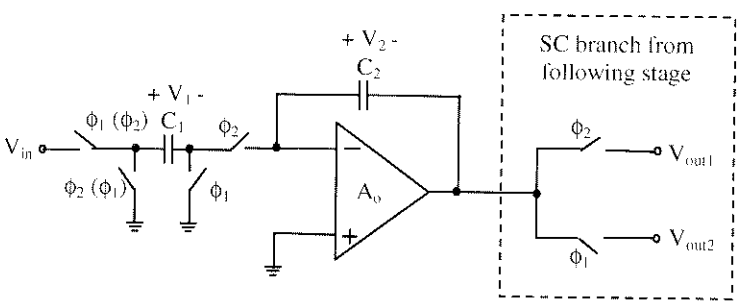


Figure 2.6 Parasitic-Insensitive Switched-Capacitor Integrators

The stray-insensitive SC integrator can be further categorized into two different types: inverting SC integrator (operates with non-parenthesized clock phases) and non-inverting SC integrator (operates with parenthesized clock phases). Since the output V_{out1} of the integrator is collected by the following SC circuit during the integration phase while the output V_{out2} is collected after the integration phase, in the z-domain, $V_{out2}(z)= z^{-1/2}V_{out1}(z)$, where $z^{-1/2}$ represents a half delay.

To analyze the finite-opamp-gain effects of the non-inverting SC integrator, the opamp is assumed to be ideal except with a finite DC gain of A_o, while all capacitors and switches are considered perfect. Table 2.2 is constructed to perform the time-domain analysis [KI 95] of the non-inverting SC integrator

with V_{out1} taken as the output. Procedures of performing time-domain analysis on SC circuits are summarized in Appendix A.

Table 2.2 Timing Diagram Showing the Charge Transferring that Occurs at SC Integrators

$\phi_2 = 1, \left[\left(n - 1/2\right) T, nT \right]$	$\phi_1 = 1, \left[nT, \left(n + 1/2\right) T \right]$	Capacitor
$V_1\left[\left(n - 1/2\right) T \right] = V_{IN}\left[\left(n - 1/2\right) T \right]$	$V_1(nT) = 0 + \frac{V_{out1}(nT)}{A_o}$	C1
$V_2\left[\left(n - 1/2\right) T \right] = -\frac{V_{out1}\left[\left(n - 1/2\right) T \right]}{A_o} - V_{out1}\left[\left(n - 1/2\right) T \right]$	$V_2(nT) = -\frac{V_{out1}(nT)}{A_o} - V_{out1}(nT)$	C2

Note that: Since there is no charge transferred to the integrating capacitor during ϕ_2, therefore: $V_{out1}\left[\left(n + 1/2\right) T \right] = V_{out1}(nT) = V_{out2}\left[\left(n + 1/2\right) T \right]$

By Kirchhoff Charge Law, during $\phi_2 \rightarrow \phi_1$ transition, i.e. from time (n-1/2) to (n), the change in charge of capacitor C_1 (ΔQ_1) is equal to that of capacitor C_2 (ΔQ_2).

i.e. $\Delta Q1 = \Delta Q2$

$$\Rightarrow C_1\left[\frac{V_{out1}(nT)}{A_o} - V_{IN}\left[\left(n - 1/2\right) T\right]\right] = C_2\left[-\frac{V_{out1}(nT)}{A_o} - V_{out1}(nT) + \frac{V_{out1}[(n-1)T]}{A_o} + V_{out1}[(n-1)T]\right]$$

$$\Rightarrow C_1[V_{IN}(nT)] = -\left[\frac{C_1}{A_o} + \frac{C_2}{A_o} + C_2\right][V_{out1}(nT)] + \left[\frac{C_2}{A_o} + C_2\right][V_{out1}[(n-1)T]]$$

By z-transformation, the z-domain transfer function of the conventional non-inverting-delay SC integrator with output taken at V_{out1} during ϕ_1 is given by:

$$H_1(z) = \frac{V_{out1}(z)}{V_{IN}(z)} = \frac{C_1 z^{-1/2}}{\left[\frac{C_1 + C_2}{A_o} + C_2\right] - \left[\frac{C_2}{A_o} + C_2\right] z^{-1}}$$

The ideal transfer function of the non-inverting-delay SC integrator with infinite opamp gain is given by:

$$H_{Ideal}(z)=\frac{V_{out1}(z)}{V_{IN}(z)}=\frac{C_1 z^{-1/2}}{C_2\left(1-z^{-1}\right)}$$

It can be observed that the gain of the integrator has been reduced from C_1/C_2 to a smaller value due to the finite opamp gain. Also, the pole has now a smaller positive value. To investigate the finite-opamp-gain effects to the frequency response of the integrator, the transfer function of the integrator is written in term of the ideal transfer function [GRE 86]:

$$\frac{H_{Ideal}(z)}{H_1(z)}=\frac{\left[\frac{C_1+C_2}{A_o}+C_2\right]-\left[\frac{C_2}{A_o}+C_2\right]z^{-1}}{C_2\left(1-z^{-1}\right)}$$

$$\Rightarrow H_1\left(e^{j\omega T}\right)=\frac{H_{Ideal}\left(e^{j\omega T}\right)}{1+\left(\frac{1+C_1/2C_2}{A_o}\right)-j\left(\frac{C_1/2C_2}{A_o\tan\left(\frac{\omega T}{2}\right)}\right)}$$

$$=\frac{H_{Ideal}\left(e^{j\omega T}\right)}{1-m(\omega)-j\theta(\omega)}=F(\omega)H_{Ideal}\left(e^{j\omega T}\right)$$

where

$$m(\omega)=-\frac{1}{A_o}\left(1+\frac{C_1}{2C_2}\right)$$

$$\theta(\omega)=\frac{C_1/C_2}{2A_o\tan\left(\frac{\omega T}{2}\right)}\approx\frac{C_1/C_2}{A_o\omega T}$$

The error factor F(ω) introduced by the finite-opamp-gain effects into the frequency response of the inverting SC integrator can be written in the polar form:

$$F(\omega)=|F(\omega)|e^{j\angle F(\omega)}$$

where

$$|F(\omega)|^2 = \frac{1}{[1-m(\omega)]^2 + [\theta(\omega)]^2} \approx \left[\frac{1}{1-m(\omega)}\right]^2 \approx [1+m(\omega)]^2$$

and

$$\angle F(\omega) = -\tan^{-1}\left[\frac{-\theta(\omega)}{1-m(\omega)}\right] \approx \tan^{-1}\theta(\omega) \approx \theta(\omega)$$

$$\Rightarrow F(\omega) \approx [1+m(\omega)]e^{j\theta(\omega)} = \left[1-\frac{1}{A_o}\left(1+\frac{C_1}{2C_2}\right)\right] e^{j\left(\frac{C_1/C_2}{A_o\omega T}\right)}$$

Thus, m(ω) represents the relative magnitude error, while θ(ω) the phase error in radians caused by the finite-opamp-gain effects. Considering when the integrator is operating at its unity-gain frequency ω_i, at which

$$H_{Ideal}\left(e^{j\omega_i T}\right) = 1$$

$$\Rightarrow \frac{C_1}{C_2} = 2\sin\left(\frac{\omega_i T}{2}\right)$$

$$\Rightarrow m(\omega_i) = -\frac{1}{A_o}\left[1+\sin\left(\frac{\omega_i T}{2}\right)\right]$$

For $\omega_i << \omega_s$, where ω_s is the sampling frequency of the circuit,

$$\Rightarrow \sin\left(\frac{\omega_i T}{2}\right) \approx 0$$

$$\Rightarrow m(\omega_i) \approx -\frac{1}{A_o}$$

and

$$\theta(\omega_i) = \frac{1}{A_o}\cos\left(\frac{\omega_i T}{2}\right) \approx \frac{1}{A_o}$$

Implications: The magnitude error m(ω) can be regarded as the deviation of the designed gain of the integrator C_1/C_2 from its nominal value by a relative error of $1/A_o$, while the finite opamp gain also introduces a relative phase error of $1/A_o$.

Considering the conventional non-inverting SC integrator with output taken at V_{out2} during ϕ_1, the transfer function is given by:

$$H_2(z) = \frac{V_{out2}(z)}{V_{IN}(z)} = \frac{C_1 z^{-1}}{\left[\frac{C_1 + C_2}{A_o} + C_2\right] - \left[\frac{C_2}{A_o} + C_2\right] z^{-1}} = H_1(z) z^{-1/2}$$

The transfer function is different from the one taken at V_{out1} only by a half delay $z^{-1/2}$. The ideal transfer function of the inverting SC integrator with infinite opamp gain is given by:

$$H_{ideal}(z) = \frac{V_{out2}(z)}{V_{IN}(z)} = \frac{C_1 z^{-1}}{C_2(1 - z^{-1})}$$

The full delay z^{-1} is cancelled when writing the actual transfer function $H_2(z)$ in term of its ideal equation. As a result, the sensitivity to finite opamp gain of the non-inverting SC integrator is the same no matter at which clock phase its output is taken. Lastly, it could be easily shown that the error factor $F(\omega)$ introduced by the finite-opamp-gain effects into the frequency response of the inverting SC integrator is identical to that of the non-inverting SC integrator. The complete analysis is shown in Appendix B.

2.6.2 Analysis of Parasitic-Insensitive Integrators Using Original Switched-Opamp Technique

Figure 2.7 shows the schematic of a non-inverting half-delay switched-capacitor integrator using the original switched-opamp technique. To analyze the finite-opamp-gain effects of this integrator, the opamp is assumed to be ideal except with a finite DC gain of A_o while all capacitors and switches are considered perfect.

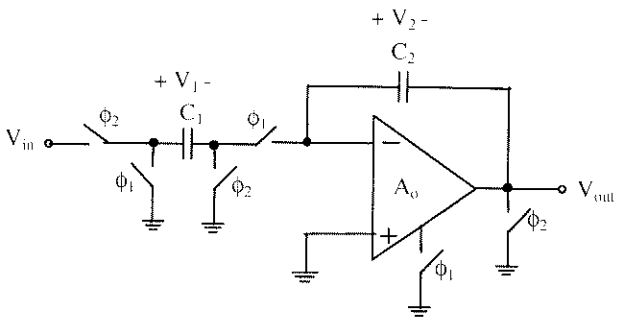


Figure 2.7 Non-Inverting SC Integrator Using Original Switched-Opamp Technique

Table 2.3 is constructed to perform the time-domain analysis of the inverting SC integrator with output V_{out} at ϕ_1. Since the opamp is turned off after integration phase ϕ_1, the output signal is only available during ϕ_1.

Table 2.3 Timing Diagram Showing the Charge Transferring that Occurs at Half-Delay Non-Inverting Switched-Opamp Integrator

$\phi_2 = 1, \left[\left(n - \frac{1}{2}\right) T, nT \right]$	$\phi_1 = 1, \left[nT, \left(n + \frac{1}{2}\right) T \right]$	Cap.
$V_1\left[\left(n - \frac{1}{2}\right) T \right] = 0$	$V_1(nT) = V_{IN}(nT) + \frac{V_{out1}(nT)}{A_o}$	C1
$V_2\left[\left(n - \frac{1}{2}\right) T \right] = -\frac{V_{out1}\left[\left(n - \frac{1}{2}\right) T \right]}{A_o} - V_{out1}\left[\left(n - \frac{1}{2}\right) T \right]$	$V_2(nT) = -\frac{V_{out1}(nT)}{A_o} - V_{out1}(nT)$	C2

Though the opamp output V_{out} is shorted to ground when the opamp is turned off after its integration phase, the information stored in the integrating capacitor C_2 is not discharged. As a result, this non-inverting half-delay switched-opamp integrator would have the z-domain transfer function as given below:

$$H_1(z) = \frac{V_{out1}(z)}{V_{IN}(z)} = \frac{-C_1 z^{-1/2}}{\left[\frac{C_1 + C_2}{A_o} + C_2\right] - \left[\frac{C_2}{A_o} + C_2\right] z^{-1}}$$

which is as same as that of the conventional non-inverting SC integrator with output (V_{out1}) taken at the end of its integration phase ϕ_1. As a result, it also has the same sensitivity to the finite opamp gain as that of the conventional non-inverting SC integrator, as given below:

$$m(\omega) = -\frac{1}{A_o}\left(1 + \frac{C_1}{2C_2}\right)$$

$$\theta(\omega) = \frac{C_1/C_2}{2A_o \tan\left(\frac{\omega T}{2}\right)} \approx \frac{C_1/C_2}{A_o \omega T}$$

where $m(\omega)$ and $\theta(\omega)$ represent respectively the relative magnitude error and the phase error in radians caused by the finite-opamp-gain effects.

Considering when the integrator is operating at its unity-gain frequency ω_i, we have

$$m(\omega_i) \approx -\frac{1}{A_o} \quad and \quad \theta(\omega_i) \approx \frac{1}{A_o}$$

Again, the magnitude error $m(\omega_i)$ can be regarded as the deviation of the designed gain of the integrator C_1/C_2 from its nominal value by a relative error of $1/A_o$, while the finite opamp gain also introduces a relative phase error of $1/A_o$. It is obvious that the performance of the half-delay non-inverting SC integrator is not degraded when implemented with the original switched-opamp technique. Nevertheless, since the output signal is not available after the integration phase, additional half-delay element has to be employed to realize the full-delay non-inverting SC integrator, which is shown in Fig. 2.8 below:

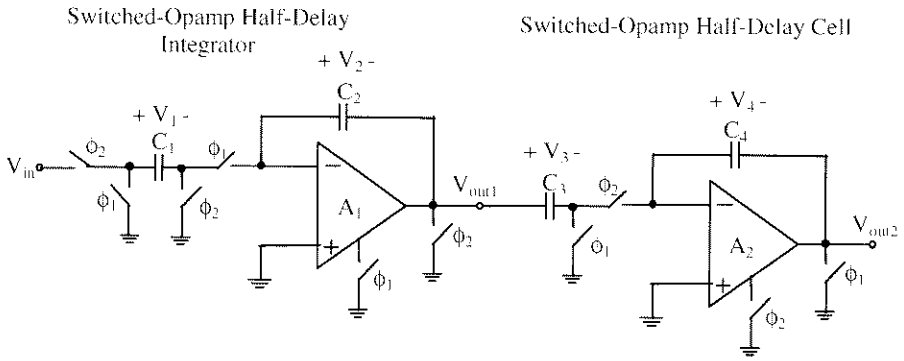


Figure 2.8 Full-Delay Non-Inverting SC Integrator Using Original Switched-Opamp Technique

To analyze the finite-opamp-gain-effects of this integrator, the opamp is assumed to be ideal except with a finite DC gain of A_o while all capacitors and switches are considered perfect. Capacitors C_3 and C_4 are considered identical to realize a unity-gain half-delay function. Obviously, the switched-opamp half-delay cell introduces additional error to the integrator. Table 2.4 is constructed to perform the time-domain analysis of the SC half-delay cell.

Table 2.4 Timing Diagram Showing the Charge Transferring that Occurs at Half-Delay Cell

$\phi_1 = 1, \left[nT, \left(n + \frac{1}{2}\right) T \right]$	$\phi_2 = 1, \left[\left(n + \frac{1}{2}\right) T, (n+1)T \right]$	Cap.
$V_3(nT) = V_{out1}(nT)$	$V_3[(n+1/2)T] = 0 - \left[-\frac{V_{out2}[(n+1/2)T]}{A_2} \right]$	C3
$V_4(nT) = 0$	$V_4\left[\left(n+\frac{1}{2}\right)T\right] = -\frac{V_{out2}\left[\left(n+\frac{1}{2}\right)T\right]}{A_2} - V_{out2}\left[\left(n+\frac{1}{2}\right)T\right]$	C4

By Kirchhoff Charge Law, during $\phi_1 \rightarrow \phi_2$ transition, i.e. from time (n) to (n+1/2), the change in charge of capacitor C_3 (ΔQ_3) is equal to that of capacitor C_4 (ΔQ_4).

$$i.e.\ \Delta Q3 = \Delta Q4$$

$$\Rightarrow C_3\left[V_{out1}(nT) - \frac{V_{out2}\left[\left(n+\frac{1}{2}\right)T\right]}{A_2}\right] = C_4\left[0 - \frac{V_{out2}\left[\left(n+\frac{1}{2}\right)T\right]}{A_2} + V_{out2}\left[\left(n+\frac{1}{2}\right)T\right]\right]$$

$$\Rightarrow C_3[V_{out1}(nT)] = C_4\left[1+\frac{2}{A_2}\right]\left[V_{out2}\left[\left(n+\frac{1}{2}\right)T\right]\right]$$

$$\xrightarrow{z\text{-}transformation}$$

$$H_{delay-cell}(z) = \frac{V_{out2}(z)}{V_{out1}(z)} = \frac{C_3 z^{-1/2}}{C_4\left[1+\frac{2}{A_2}\right]}$$

The ideal transfer function of the unity-gain SC half-delay cell with infinite opamp gain is given by:

$$H_{Ideal}(z) = \frac{V_{out2}(z)}{V_{Iout1}(z)} = z^{-1/2}$$

It can be observed that the gain of the SC half-delay cell has been reduced from C_3/C_4 to a smaller value due to the finite opamp gain. To investigate the finite-opamp-gain effects to the frequency response of the integrator, the transfer function of the integrator is written in term of the ideal transfer function:

$$\frac{H_{Ideal}(z)}{H_{delay-cell}(z)} = \frac{z^{-1/2}}{\frac{C_3 z^{-1/2}}{C_4\left[1+\frac{2}{A_2}\right]}} = \frac{C_4\left[1+\frac{2}{A_2}\right]}{C_3}$$

Substituting $z = e^{j\omega T}$,

$$H_{delay-cell}\left(e^{j\omega T}\right) = \frac{H_{Ideal}\left(e^{j\omega T}\right)}{\frac{C_3}{C_4}\left(\frac{1}{1+\frac{2}{A_2}}\right)} = \frac{H_{Ideal}\left(e^{j\omega T}\right)}{1-m(\omega)-j\theta(\omega)} = F(\omega)H_{Ideal}\left(e^{j\omega T}\right)$$

where

$$m(\omega) = \frac{C_3}{C_4}\left(\frac{1}{1+\frac{2}{A_2}}\right) - 1$$

$$\theta(\omega) = 0$$

The error factor $F(\omega)$ introduced by the finite-opamp-gain effects into the frequency response of the inverting SC integrator can be written in the polar form:

$$F(\omega) = |F(\omega)|e^{j\angle F(\omega)}$$

where

$$|F(\omega)|^2 = \frac{1}{[1-m(\omega)]^2+[\theta(\omega)]^2} \approx \left[\frac{1}{1-m(\omega)}\right]^2 \approx [1+m(\omega)]^2$$

and

$$\angle F(\omega) = -\tan^{-1}\left[\frac{-\theta(\omega)}{1-m(\omega)}\right] \approx \tan^{-1}\theta(\omega) \approx \theta(\omega) = 0$$

$$\Rightarrow F(\omega) \approx [1+m(\omega)]e^{j\theta(\omega)} = \frac{C_3}{C_4}\left(\frac{1}{1+\frac{2}{A_2}}\right) \approx \frac{C_3}{C_4}\left(1-\frac{2}{A_2}\right)$$

Thus, due to the finite opamp gain, the SC half-delay cell only introduces a relative magnitude error of m(ω) but not phase error. The overall sensitivity of the switched-opamp full-delay integrator is given by:

$$F_{Overall}(\omega) = \left[\left|F_{half-delay-\text{int}egrator}(\omega)\right|\left|F_{delay-cell}(\omega)\right|\right]e^{j\left[\angle F_{half-delay-\text{int}egrator}(\omega)+\angle F_{delay-cell}(\omega)\right]}$$

$$\Rightarrow F_{Overall}(\omega) = \left[1-\frac{1}{A_1}\left(1+\frac{C_1}{2C_2}\right)\right]\left(\frac{C_3}{C_4}\right)\left(1-\frac{2}{A_2}\right)e^{j\left(\frac{C_1/C_2}{A_1\omega T}\right)}$$

$$\approx \left[1-\frac{2}{A_2}-\frac{1}{A_1}\left(1+\frac{C_1}{2C_2}\right)\right]\left(\frac{C_3}{C_4}\right)e^{j\left(\frac{C_1/C_2}{A_1\omega T}\right)}$$

If $A_1 = A_2$,

$$\Rightarrow F_{Overall}(\omega) \approx \left[1-\frac{1}{A_1}\left(3+\frac{C_1}{2C_2}\right)\right]\left(\frac{C_3}{C_4}\right)e^{j\left(\frac{C_1/C_2}{A_1\omega T}\right)}$$

Considering when the integrator is operating at its unity-gain frequency ω_i and capacitors C_3 and C_4 are identical, this implies

$$H_{Ideal}\left(e^{j\omega_i T}\right) = 1$$

$$\Rightarrow \frac{C_1}{C_2} = 2\sin\left(\frac{\omega_i T}{2}\right)$$

$$\Rightarrow m(\omega_i) = -\frac{1}{A_1}\left[3+\sin\left(\frac{\omega_i T}{2}\right)\right]$$

For $\omega_i << \omega_s$, where ω_s is the sampling frequency of the circuit,

$$\Rightarrow \sin\left(\frac{\omega_i T}{2}\right) \approx 0$$

$$\Rightarrow m(\omega_i) \approx -\frac{3}{A_o}$$

and

$$\theta(\omega_i) = \frac{1}{A_o}\cos\left(\frac{\omega_i T}{2}\right) \approx \frac{1}{A_o}$$

Implications: The magnitude error $m(\omega)$ can be regarded as the deviation of the designed gain of the integrator C_1/C_2 from its nominal value by a relative error of $3/A_o$, while the finite opamp gain also introduces a relative phase error of $1/A_o$. Though the SC half-delay cell does not introduce additional phase error to the overall integrator response, the magnitude error is increased three times. As a result, the minimum opamp gain requirement of those SC circuits that employ such a full-delay switched-opamp integrator would be higher in order to preserve the amplitude response.

Similarly, the original switched-opamp can be employed to realize the inverting SC integrator. However, since the output signal is not available after the integration phase ϕ_1, only non-delay inverting switched-opamp integrator can be implemented with the original switched-opamp technique unless additional SC half-delay cell is employed. It could be shown that the performance of the non-delay inverting SC integrator is not degraded when implemented with the original switched-opamp technique. Nevertheless, additional half-delay element has to be employed to realize the half-delay version of the inverting SC integrator due to the switch-off of the opamp after the integration phase. As a result, the magnitude error is increased by three times. Since the analysis of this switched-opamp integrator is the same as the conventional inverting integrator, it is not repeated here.

2.6.3 Analysis of Parasitic-Insensitive Integrators Using Multi-Phase Switched-Opamp Technique

Figure 2.9 shows the schematic of a non-inverting full-delay switched-capacitor integrator implemented with the multi-phase switched-opamp technique. Two opamps with finite DC gain of A_1 and A_2 are operated alternately at ϕ_1 and ϕ_2 respectively. To analyze the finite-opamp-gain effects of this integrator, the opamps are assumed to be ideal except with finite DC gain while all capacitors and switches are considered perfect. Specially, capacitors C_2 and C_3 are assumed identical. This non-inverting switched-

opamp integrator functions as a full-delay integrator when the output V_{out2} is taken. Table 2.5 is constructed to perform the time-domain analysis.

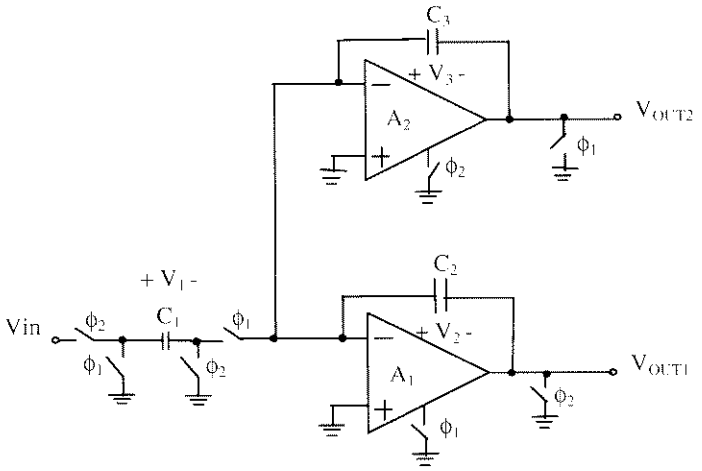


Figure 2.9 Full-Delay Non-Inverting SC Integrator Using Multi-Phase Switched-Opamp Technique

Table 2.5 Timing Diagram Showing the Charge Transferring that Occurs at Full-Delay Non-Inverting Switched-Opamp Integrator

$\phi_2 \rightarrow \phi_1$	$\phi_2 \rightarrow \phi_1$		
$\phi_2 = 1, \left[\left(n - \frac{1}{2}\right)T, nT\right]$	$\phi_1 = 1, \left[nT, \left(n + \frac{1}{2}\right)T\right]$	$\phi_2 = 1, \left[\left(n + \frac{1}{2}\right)T, (n+1)T\right]$	
$V_1\left[\left(n - \frac{1}{2}\right)T\right] = V_{IN}\left[\left(n - \frac{1}{2}\right)T\right]$	$V_1(nT) = 0 - \left[-\frac{V_{out1}(nT)}{A_1}\right]$	$V_1\left[\left(n + \frac{1}{2}\right)T\right] = V_{IN}\left[\left(n + \frac{1}{2}\right)T\right]$	C_1
$V_2\left[\left(n - \frac{1}{2}\right)T\right] = -\frac{V_{out2}\left[\left(n - \frac{1}{2}\right)T\right]}{A_2}$	$V_2(nT) = -\frac{V_{out1}(nT)}{A_1} - V_{out1}(nT)$	$V_2\left[\left(n + \frac{1}{2}\right)T\right] = -\frac{V_{out2}\left[\left(n + \frac{1}{2}\right)T\right]}{A_2}$	C_2
$V_3\left[\left(n - \frac{1}{2}\right)T\right] = -\frac{V_{out2}\left[\left(n - \frac{1}{2}\right)T\right]}{A_2} - V_{out2}\left[\left(n - \frac{1}{2}\right)T\right]$	$V_3(nT) = -\frac{V_{out1}(nT)}{A_1}$	$V_3\left[\left(n + \frac{1}{2}\right)T\right] = -\frac{V_{out2}\left[\left(n + \frac{1}{2}\right)T\right]}{A_2} - V_{out2}\left[\left(n + \frac{1}{2}\right)T\right]$	C_3

By Kirchhoff Charge Law, during $\phi_1 \rightarrow \phi_2$ transition, i.e. from time (n)T to (n+1/2)T, there is no charge transfer from capacitor C_1 to the opamp. Thus the net change in charge of capacitors C_2 (ΔQ_2) and C_3 (ΔQ_3) are null.

i.e. $\Delta Q2 + \Delta Q3 = 0$

$$\Rightarrow C_2\left[-\frac{V_{out2}\left[\left(n+1/2\right)T\right]}{A_2}+\frac{V_{out1}(nT)}{A_1}+V_{out1}(nT)\right]$$

$$+C_3\left[-\frac{V_{out2}\left[\left(n+1/2\right)T\right]}{A_2}-V_{out2}\left[\left(n+1/2\right)T\right]+\frac{V_{out1}(nT)}{A_1}\right]=0$$

$$\Rightarrow\left[\frac{C_2}{A_1}+C_2+\frac{C_3}{A_1}\right]\left[V_{out1}(nT)\right]-\left[\frac{C_2}{A_2}+\frac{C_3}{A_2}+C_3\right]\left[V_{out2}\left[\left(n+1/2\right)T\right]\right]=0$$

By z-transformation, the outputs V_{out1} and V_{out2} are related in the z-domain by:

$$\frac{V_{out1}(z)}{V_{out2}(z)}=\left[\frac{\left(C_3+\frac{C_2+C_3}{A_2}\right)}{\left(C_2+\frac{C_2+C_3}{A_1}\right)}\right]z^{1/2} \qquad \text{(Eq. 2.2)}$$

With matched capacitors C_2 and C_3 and matched gain of opamps A_1 and A_2, V_{out2} is just a duplication of V_{out1} but delayed by half a clock cycle. It should be emphasized that the actual gain of the opamps is not important to maintain the quality of this equation.

During $\phi_2 \rightarrow \phi_1$ transition, i.e. from time (n-1/2) to (n), the change in charge of capacitor C_1 (ΔQ_1) is equal to the sum of that of capacitor C_2 (ΔQ_2) and C_3 (ΔQ_3).

i.e. $\Delta Q1 = \Delta Q2 + \Delta Q3$

$$\Rightarrow C_1\left[\frac{V_{out1}(nT)}{A_1} - V_{IN}\left[\left(n-\tfrac{1}{2}\right)T\right]\right] = C_2\left[-\frac{V_{out1}(nT)}{A_1} - V_{out1}(nT) + \frac{V_{out2}\left[\left(n-\tfrac{1}{2}\right)T\right]}{A_2}\right]$$

$$+ C_3\left[-\frac{V_{out1}(nT)}{A_1} + \frac{V_{out2}\left[\left(n-\tfrac{1}{2}\right)T\right]}{A_2} + V_{out2}\left[\left(n-\tfrac{1}{2}\right)T\right]\right]$$

$$\Rightarrow -C_1\left[V_{IN}\left[\left(n-\tfrac{1}{2}\right)T\right]\right]$$

$$= -\left[\frac{C_1}{A_1} + \frac{C_2}{A_1} + C_2 + \frac{C_3}{A_1}\right]\left[V_{out1}(nT)\right] + \left[\frac{C_2}{A_2} + \frac{C_3}{A_2} + C_3\right]\left[V_{out2}\left[\left(n-\tfrac{1}{2}\right)T\right]\right]$$

$\xrightarrow{Z\text{-}transformation}$

$$\Rightarrow -C_1[V_{IN}(z)]z^{-1/2}$$

$$= -\left[C_2 + \frac{C_1 + C_2 + C_3}{A_1}\right][V_{out1}(z)] + \left[\frac{C_2 + C_3}{A_2} + C_3\right][V_{out2}(z)]\ z^{-1/2} \qquad \text{(Eq. 2.3)}$$

Substituting Equation 2.2 into Equation 2.3, the z-domain transfer function of the integrator with V_{out2} taken as the output is given by:

$$\Rightarrow C_1[V_{IN}(z)]z^{-1/2} = \left[\frac{C_3 + \frac{C_2 + C_3}{A_2}}{C_2 + \frac{C_2 + C_3}{A_1}}\right]\left[C_2 + \frac{C_1 + C_2 + C_3}{A_1}\right][V_{out2}(z)]\ z^{1/2}$$

$$- \left[\frac{C_2 + C_3}{A_2} + C_3\right][V_{out2}(z)]\ z^{-1/2}$$

$$\Rightarrow C_1[V_{IN}(z)]z^{-1}$$

$$= \left\{\left[\frac{C_3 + \frac{C_2 + C_3}{A_2}}{C_2 + \frac{C_2 + C_3}{A_1}}\right]\left[C_2 + \frac{C_1 + C_2 + C_3}{A_1}\right] - \left[\frac{C_2 + C_3}{A_2} + C_3\right]\ z^{-1}\right\}[V_{out2}(z)]$$

$$\Rightarrow H(z)=\frac{V_{out2}(z)}{V_{IN}(z)}=\frac{C_1 z^{-1}}{\left[\frac{C_3+\frac{C_2+C_3}{A_2}}{C_2+\frac{C_2+C_3}{A_1}}\right]\left[C_2+\frac{C_1+C_2+C_3}{A_1}\right]-\left[\frac{C_2+C_3}{A_2}+C_3\right]z^{-1}}$$

Assume $C_2 \equiv C_3 \equiv C$,

$$\Rightarrow H(z)=\frac{V_{out2}(z)}{V_{IN}(z)}=\frac{C_1 z^{-1}}{C\left[\left(\frac{1+\frac{2}{A_2}}{1+\frac{2}{A_1}}\right)\left(1+\frac{C_1/C+2}{A_1}\right)-\left(1+\frac{2}{A_2}\right)z^{-1}\right]}$$

The ideal transfer function of the non-inverting full-delay SC integrator with infinite opamp gain is given by:

$$H_{Ideal}(z)=\frac{V_{out2}(z)}{V_{IN}(z)}=\frac{C_1 z^{-1}}{C\left(1-z^{-1}\right)}$$

It can be observed that the gain of the integrator has been reduced from C_1/C to a smaller value due to the finite opamp gain. Also, the pole has now a smaller positive value. To investigate the finite-opamp-gain effects to the frequency response of the integrator, the transfer function of the integrator is written in term of the ideal transfer function:

$$\frac{H_{Ideal}(z)}{H_1(z)}=\frac{\left(\frac{1+\frac{2}{A_2}}{1+\frac{2}{A_1}}\right)\left(1+\frac{C_1/C+2}{A_1}\right)-\left(1+\frac{2}{A_2}\right)z^{-1}}{1-z^{-1}}$$

$$\approx\frac{\left(1+\frac{2}{A_2}\right)\left(1-\frac{2}{A_1}\right)\left(1+\frac{C_1/C+2}{A_1}\right)-\left(1+\frac{2}{A_2}\right)z^{-1}}{1-z^{-1}}$$

$$\approx \frac{\left[1+2\left(\frac{1}{A_2}-\frac{1}{A_1}\right)\right]\left(1+\frac{C_1/C+2}{A_1}\right)-\left(1+\frac{2}{A_2}\right)z^{-1}}{1-z^{-1}}$$

$$\approx \frac{\left[1+2\left(\frac{1}{A_2}-\frac{1}{A_1}\right)+\frac{C_1/C+2}{A_1}\right]-\left(1+\frac{2}{A_2}\right)z^{-1}}{1-z^{-1}}$$

$$= \frac{\left(1+\frac{2}{A_2}+\frac{C_1/C}{A_1}\right)-\left(1+\frac{2}{A_2}\right)z^{-1}}{1-z^{-1}}$$

$$= \frac{1+\left[1+\left(\frac{A_2}{2}\right)\left(\frac{C_1/C}{A_1}\right)\right]\left(\frac{2}{A_2}\right)-\left(1+\frac{2}{A_2}\right)z^{-1}}{1-z^{-1}}$$

$$\frac{\left\{1+\left[1+\left(\frac{1}{2}\right)\left(\frac{A_2}{2}\right)\left(\frac{C_1/C}{A_1}\right)\right]\left(\frac{2}{A_2}\right)\right\}+\left(\frac{1}{2}\right)\left(\frac{C_1/C}{A_1}\right)-\left\{1+\left[1+\left(\frac{1}{2}\right)\left(\frac{A_2}{2}\right)\left(\frac{C_1/C}{A_1}\right)\right]\left(\frac{2}{A_2}\right)\right\}z^{-1}+\left(\frac{1}{2}\right)\left(\frac{C_1/C}{A_1}\right)z^{-1}}{1-z^{-1}}$$

$$1+\left[1+\left(\frac{1}{2}\right)\left(\frac{A_2}{2}\right)\left(\frac{C_1/C}{A_1}\right)\right]\left(\frac{2}{A_2}\right)+\left(\frac{C_1/C}{2A_1}\right)\left(\frac{1+z^{-1}}{1-z^{-1}}\right)$$

Substituting $z = e^{j\omega T}$,

$$\frac{H_{Ideal}\left(e^{j\omega T}\right)}{H\left(e^{j\omega T}\right)} = 1 + \left[1 + \left(\frac{C_1/C}{A_1}\right)\left(\frac{A_2}{2}\right)\right]\left(\frac{1}{A_2}\right) + \left(\frac{C_1/C}{2A_1}\right)\left(\frac{e^{\frac{j\omega T}{2}} + e^{\frac{-j\omega T}{2}}}{e^{\frac{j\omega T}{2}} - e^{\frac{-j\omega T}{2}}}\right)$$

$$= 1 + \left[1 + \left(\frac{C_1/C}{A_1}\right)\left(\frac{A_2}{2}\right)\right]\left(\frac{1}{A_2}\right) - j\left(\frac{C_1/C}{2A_1 \tan\left(\frac{\omega T}{2}\right)}\right)$$

$$\Rightarrow H\left(e^{j\omega T}\right) = \frac{H_{Ideal}\left(e^{j\omega T}\right)}{1 + \left[1 + \left(\frac{C_1/C}{A_1}\right)\left(\frac{A_2}{2}\right)\right]\left(\frac{1}{A_2}\right) - j\left(\frac{C_1/2C}{A_o \tan\left(\frac{\omega T}{2}\right)}\right)}$$

$$= \frac{H_{Ideal}\left(e^{j\omega T}\right)}{1 - m(\omega) - j\theta(\omega)} = F(\omega) H_{Ideal}\left(e^{j\omega T}\right)$$

where

$$m(\omega) = -\frac{1}{A_2}\left[1 + \left(\frac{C_1/C}{A_1}\right)\left(\frac{A_2}{2}\right)\right]$$

$$\theta(\omega) = \frac{C_1/C}{2A_1 \tan\left(\frac{\omega T}{2}\right)} \approx \frac{C_1/C}{A_1 \omega T}$$

The error factor F(ω) introduced by the finite opamp gain into the frequency response of the inverting SC integrator can be written in the polar form:

$$F(\omega) = |F(\omega)| e^{j\angle F(\omega)}$$

where

$$|F(\omega)|^2 = \frac{1}{[1-m(\omega)]^2 + [\theta(\omega)]^2} \approx \left[\frac{1}{1-m(\omega)}\right]^2 \approx [1+m(\omega)]^2$$

and

$$\angle F(\omega) = -\tan^{-1}\left[\frac{-\theta(\omega)}{1-m(\omega)}\right] \approx \tan^{-1}\theta(\omega) \approx \theta(\omega)$$

$$\Rightarrow F(\omega) \approx [1+m(\omega)]e^{j\theta(\omega)} = \left[1-\frac{1}{A_2}\left[1+\left(\frac{C_1/C}{A_1}\right)\left(\frac{A_2}{2}\right)\right]\right] e^{j\left(\frac{C_1/C}{A_1\omega T}\right)}$$

Thus, m(ω) represents the relative magnitude error, while θ(ω) the phase error in radians caused by the finite-gain effect. Considering when the integrator is operating at its unity-gain frequency ω_i, at which

$$H_{Ideal}\left(e^{j\omega_i T}\right) = 1$$

$$\Rightarrow \frac{C_1}{C} = 2\sin\left(\frac{\omega_i T}{2}\right)$$

$$\Rightarrow m(\omega_i) = -\frac{1}{A_2}\left[1+\sin\left(\frac{\omega_i T}{2}\right)\right]$$

For $\omega_i << \omega_s$, where ω_s is the sampling frequency of the circuit,

$$\Rightarrow \sin\left(\frac{\omega_i T}{2}\right) \approx 0$$

$$\Rightarrow m(\omega_i) \approx -\frac{1}{A_2}$$

and

$$\theta(\omega_i) = \frac{1}{A_2}\cos\left(\frac{\omega_i T}{2}\right) \approx \frac{1}{A_2}$$

Implications: The magnitude error m(ω) can be regarded as the deviation of the designed gain of the integrator C_1/C from its nominal value by a relative error of $1/A_2$, while the finite-opamp-gain also introduces a relative phase error of $1/A_2$. This is interesting to point out that both of the magnitude and phase errors, at the unity-gain frequency, of the integrator is independent to the finite opamp gain of opamp A_1. Consequently, if V_{out1} is the only interested output to be taken, the integrator is operating as a half-delay non-inverting SC integrator, which requires only one opamp (A_1) for the realization as described in section 2.6.1. Nevertheless, being implemented with the multi-phase switched-opamp technique, the inclusion of opamp A_2 could still implement the half-delay non-inverting SC integrator by accessing the output V_{out1}. Substituting Equation 2.2 into Equation 2.3 to extract the transfer function between $V_{out1}(z)$ and Vin(z):

$$\Rightarrow C_1[V_{IN}(z)]z^{-1/2} = \left[C_2 + \frac{C_1 + C_2 + C_3}{A_1}\right][V_{out1}(z)] - \left[\frac{C_2 + C_3}{A_2} + C_3\right]\left[\frac{C_2 + \frac{C_2 + C_3}{A_1}}{C_3 + \frac{C_2 + C_3}{A_2}}\right][V_{out1}(z)]\ z^{-1}$$

$$\Rightarrow C_1[V_{IN}(z)]z^{-1/2} = \left\{\left[C_2 + \frac{C_1 + C_2 + C_3}{A_1}\right] - \left[\frac{C_2 + C_3}{A_1} + C_2\right]\ z^{-1}\right\}[V_{out1}(z)]$$

$$\Rightarrow \frac{V_{out1}(z)}{V_{in}(z)} = \frac{C_1 z^{-1/2}}{\left[C_2 + \frac{C_1 + C_2 + C_3}{A_1}\right] - \left[\frac{C_2 + C_3}{A_1} + C_2\right] z^{-1}}$$

The result shows an important implication that the transfer function of this switched-opamp integrator, where its output is taken during its integration phase, is not affected by the introduction of the additional opamp A_2, though dissipating power. This analysis can be extended to show that the additional opamp A_2 would also not affect the performance of SC pseudo-N-path cells. As a result, the sensitivity to finite opamp gain of this half-delay non-inverting switched-opamp integrator is same as that of the conventional SC implementation as well as that realized with the original switched-opamp technique as discussed previously. The magnitude and phase error at the unity-gain frequency of the integrator is given by:

$$m(\omega_i) \approx -\frac{1}{A_2}$$

and

$$\theta(\omega_i) \approx \frac{1}{A_2}$$

Lastly, since the analysis of inverting switched-opamp integrator is the same as the non-inverting integrator, it is not repeated here. It should be pointed out that the performance of both inverting and non-inverting integrators, being realized by the multi-phase switched-opamp technique, is same as the conventional SC integrators. As a result, low-voltage SC architectures employed the multi-phase switched-opamp technique could maintain low sensitivity to finite-opamp-gain effects as for the conventional SC implementation.

2.7 Performance Comparisons of Switched-Capacitor and Switched-Opamp Integrators

From the above analyses, it can be observed that multi-phase switched-opamp technique could be employed to realize all kinds of parasitic-insensitive SC integrators with same sensitivity to finite opamp gain and consume same power (need also 1 unit of opamp power). Three-time lower finite-opamp-gain sensitivity is achieved when employing multi-phase switched-opamp technique rather than the original switched-opamp technique to implement full-delay non-inverting SC integrator.

An important observation is on the realization of the half-delay non-inverting SC integrator using the original switched-opamp technique, which achieves both low sensitivity to finite opamp gain and also reduce the power consumption by 50 % as a result of the turning off of the opamp after the integration phase. Table 2.6 summarizes the sensitivity and power efficiency of the non-inverting switched-capacitor and switched-opamp integrators.

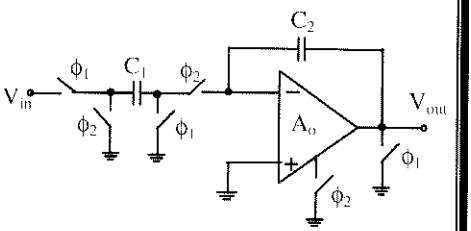
Table 2.6 Performance Summaries of Switched-Capacitor and Switched-Opamp Integrators

Non-Inverting Half-Delay Switched-Capacitor Integrators

Ideal Transfer Function of (a-c)
Realization:

$$H_{Ideal}(z)=\frac{V_{out}(z)}{V_{IN}(z)}=\frac{C_1 z^{-1/2}}{C_2\left(1-z^{-1}\right)}$$

(b) Original Switched-Opamp Integrator:



Transfer Function:

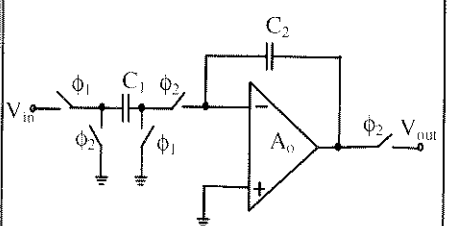
$$\frac{V_{out}(z)}{V_{IN}(z)}=\frac{C_1 z^{-1/2}}{\left[\frac{C_1+C_2}{A_o}+C_2\right]-\left[\frac{C_2}{A_o}+C_2\right]z^{-1}}$$

Magnitude Error: $\approx -\frac{1}{A_o}$

Phase Error: $\approx \frac{1}{A_o}$

Power Consumption: ½ unit of opamp power

(a) Switched-Capacitor Integrators:



Transfer Function:

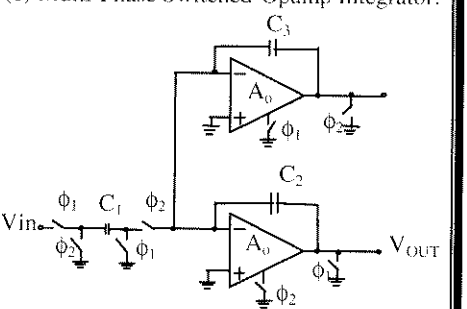
$$\frac{V_{out}(z)}{V_{IN}(z)}=\frac{C_1 z^{-1/2}}{\left[\frac{C_1+C_2}{A_o}+C_2\right]-\left[\frac{C_2}{A_o}+C_2\right]z^{-1}}$$

Magnitude Error: $\approx -\frac{1}{A_o}$

Phase Error: $\approx \frac{1}{A_o}$

Power Consumption: 1 unit opamp power

(c) Multi-Phase Switched-Opamp Integrator:



Transfer Function:

$$\frac{V_{out}(z)}{V_{in}(z)}=\frac{C_1 z^{-1/2}}{\left[C_2+\frac{C_1+C_2+C_3}{A_o}\right]-\left[\frac{C_2+C_3}{A_o}+C_2\right]z^{-1}}$$

Magnitude Error: $\approx -\frac{1}{A_o}$

Phase Error: $\approx \frac{1}{A_o}$

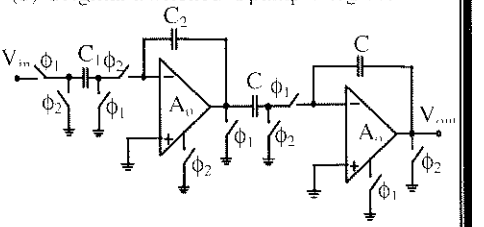
Power Consumption: 1 unit opamp power

Non-Inverting Full-Delay Switched-Capacitor Integrators

Ideal Transfer Function of (a-c) Realization:

$$H_{Ideal}(z) = \frac{V_{out}(z)}{V_{IN}(z)} = \frac{C_1 z^{-1}}{C_2\left(1 - z^{-1}\right)}$$

(b) Original Switched-Opamp Integrator:



Transfer Function:

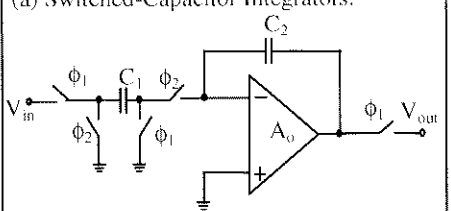
$$\frac{V_{out}(z)}{V_{IN}(z)} = \frac{C_1 z^{-1}}{\left[\frac{C_1 + C_2}{A_o} + C_2\right] - \left[\frac{C_2}{A_o} + C_2\right] z^{-1}} \left[\frac{1}{1 + \frac{2}{A_o}}\right]$$

Magnitude Error: $\approx -\frac{3}{A_o}$

Phase Error: $\approx \frac{1}{A_o}$

Power Consumption: ½ unit of opamp power

(a) Switched-Capacitor Integrators:



Transfer Function:

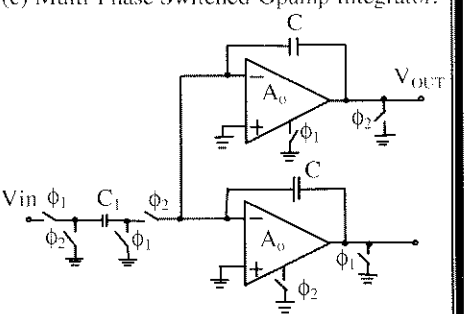
$$\frac{V_{out}(z)}{V_{IN}(z)} = \frac{C_1 z^{-1}}{\left[\frac{C_1 + C_2}{A_o} + C_2\right] - \left[\frac{C_2}{A_o} + C_2\right] z^{-1}}$$

Magnitude Error: $\approx -\frac{1}{A_o}$

Phase Error: $\approx \frac{1}{A_o}$

Power Consumption: 1 unit opamp power

(c) Multi-Phase Switched-Opamp Integrator:



Transfer Function:

$$\frac{V_{out}(z)}{V_{IN}(z)} = \frac{C_1 z^{-1}}{C\left[\left(\frac{1 + \frac{2}{A_o}}{1 + \frac{2}{A_o}}\right)\left(1 + \frac{C_1/C + 2}{A_o}\right) - \left(1 + \frac{2}{A_o}\right) z^{-1}\right]}$$

Magnitude Error: $\approx -\frac{1}{A_o}$

Phase Error: $\approx \frac{1}{A_o}$

Power Consumption: 1 unit opamp power

2.8 Conclusion

Switched-opamp techniques present a promising and reliable way to realize low-voltage switched-capacitor circuits. However, since the opamp is set inactive after the integration phase, the original switched-opamp technique causes design problems when it is applied to conventional SC systems. Multi-phase switched-opamp technique is shown to be a fully-compatible solution for low-voltage SC circuits. Nevertheless, the original switched-opamp technique, when it is applied to realize half-delay non-inverting SC integrator, could achieve 50 % power reduction while maintaining low sensitivity as the conventional SC integrators. To take advantage of the switched-opamp technique for power reduction, a family of half-delay-non-inverting-switched-capacitor-integrator-based architectures has been proposed as illustrated in next chapter.

Chapter 3

SYSTEM CONSIDERATIONS FOR HIGH-SPEED AND LOW-POWER SWITCHED-OPAMP CIRCUITS

3.1 Introduction

While circuits' performance could be increased quite linearly with the advancement of technologies, modifications and novelties in the system-level designs could achieve far more significant and pronouncing performance improvements. This chapter begins with a brief review of the double-sampling technique, which has been one of the most useful techniques in boosting the operation speed of SC circuits by double without requesting higher opamps' performance. More importantly, most of the conventional SC architectures can be directly transformed into their corresponding double-sampling architectures by duplicating a parallel path to operate alternately while maintaining the overall characteristics. However, the transformed architectures are usually not optimal in term of opamp settling consideration, which could easily waive the benefits gained by the double-sampling operation. The settling problem will be investigated by considering a conventional double-sampling SC biquadratic filter. After that, a fast-settling double-sampling SC biquadratic filter architecture will be proposed.

In the second part of this chapter, the system-level considerations for switched-opamp circuits are provided. A family of half-delay-SC-integrator-based filters and $\Sigma\Delta$ modulator has been developed to combine with switched-opamp technique for low-voltage, low-power and high-speed applications. Besides a noise-shaping-extension technique is proposed to maximize the achievable signal-to-noise-ratio for a lowpass $\Sigma\Delta$ modulator. Detailed design equations are developed.

3.2 Principle of the Double-Sampling Technique

Consider a conventional inverting SC integrator [GRE 86, P.ANA95] as shown in Fig. 3.1(a), being operated with a pair of complementary clock phases ϕ_1 and ϕ_2, the input signal is only sampled during ϕ_2 while the integrator is integrating only during ϕ_1. It is obvious that the opamp is idle during ϕ_2.

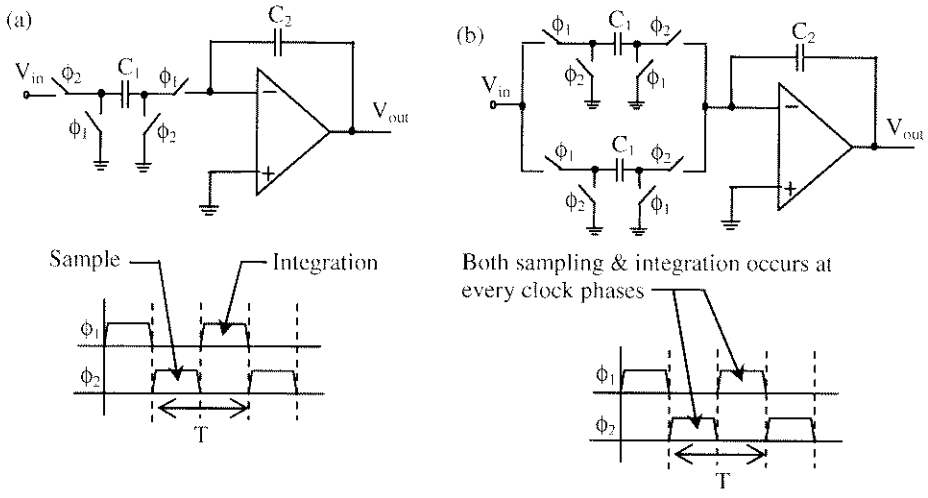


Figure 3.1 (a) Conventional Inverting SC Integrator;
(b) Double-Sampling Inverting SC Integrator

The idea of double-sampling operation is to fully utilize the opamp such that it is never idle and thus achieving double of the throughput. Figure 3.1(b) shows the configuration of the conventional inverting SC integrator in double-sampling operation. Two sampling capacitors are employed to operate alternately to sample the input signal, which is then transferred to the opamp for integration at next clock phase. As a result, the opamp is always integrating new signal at every clock phase. Since the clocking frequency is identical to the conventional SC integrator, the double-sampling technique thus effectively increases twice the sampling frequency of the circuit without requiring a higher performance opamp. It is because the opamp is still given half a clock period for settling as in the conventional SC integrator. Nevertheless, the mismatch between the two sampling paths would produce an image signal [BAZ 98, ONG 97] of the input signal. Figure 3.2 illustrates the path-mismatch effect of a double-sampling system.

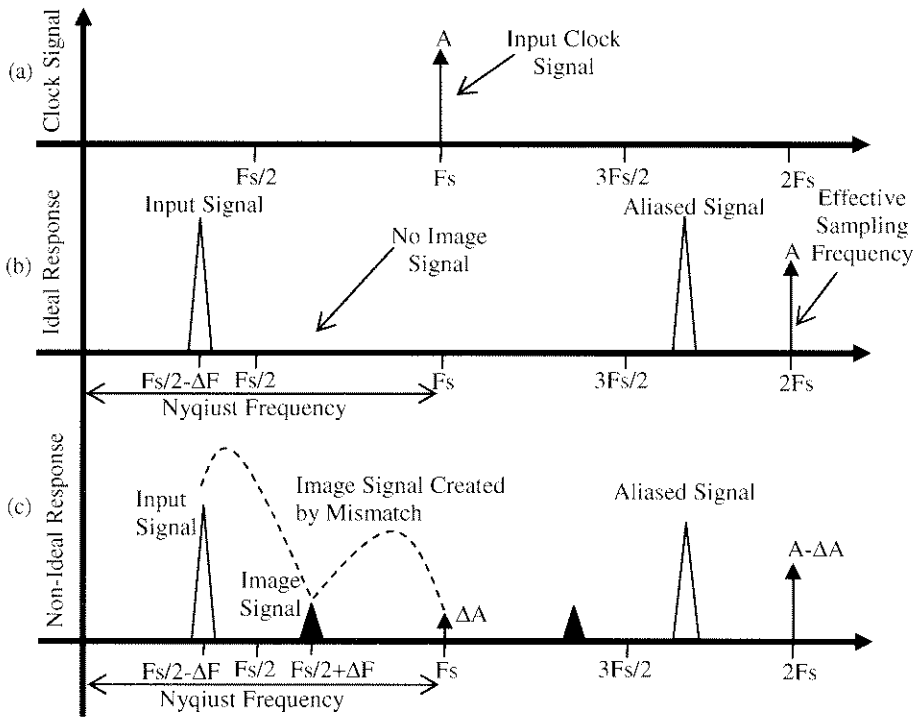


Figure 3.2 (a) Clock Signal; (b) Ideal Frequency Spectrum; (c) Non-Ideal Frequency Spectrum of a Double-Sampling System with Input Path Mismatch

Due to the path mismatch, the system experiences a sampling tone at $2F_s$ with amplitude (A-ΔA), but also another sampling tone at F_s with amplitude (ΔA), where F_s is the input clock frequency. As a result, the input signal would also alias with the sampling tone at F_s to produce its image signal. A 1-% mismatch (with good layout technique in nowadays technology) would produce an image signal 40 dB lower than the fundamental. A mismatch cancellation technique was proposed in [YU 98] to reduce the image problem, but the technique is only applicable to ΣΔ modulator topology. For systems with high image rejection requirement [GUO 01, TAD 01] (typically larger than 60 dB), the double-sampling technique may not be applicable.

3.3 Settling Problems of Opamps in Conventional Double-Sampling SC Architecture

In most of the SC systems, the double-sampling technique can be easily applied by duplicating those SC branches to operate in alternate phases, though not always optimised in term of settling problems among the opamps. Figure 3.3 depicts a typical realization of a double-sampling SC biquadratic filter architecture [NAG 97].

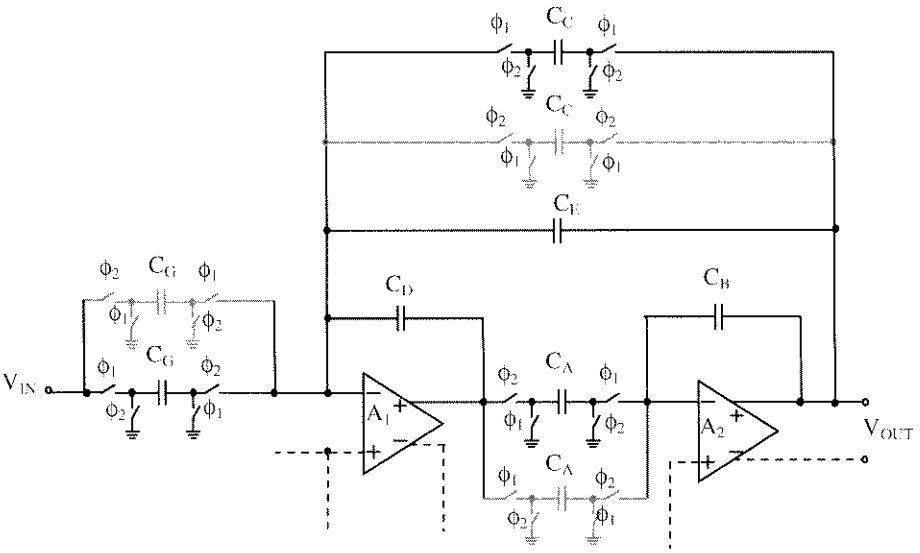


Figure 3.3 A Typical Realization of a Double-Sampled SC Biquadratic Filter

This double-sampled SC biquadratic filter architecture is derived from an E-type SC biquadratic filter [FLE 79]. The additional switched capacitors employed for double-sampling operation of the E-type biquad are drawn in grey colour. The main characteristic of the E-type SC biquad is the employment of an un-switched capacitor (C_E) as the global feedback of the system to achieve a second-order transfer function. Such a continuous capacitive feedback would lengthen the required settling time of opamp A_1, since the final output value of opamp A_1 is affected unless opamp A_2 settles. As a result, in order to achieve good settling within each clock phase (half clock period), the opamp A_1 would have to operate much faster. Besides, the upper and the lower switched capacitors C_C, which work as the input sampling capacitors of an inverting SC integrator formed by opamp A_1 and capacitor C_D, also apparently provide continuous capacitive feedback between the two opamps during ϕ_1 and ϕ_2 respectively. As a result, the settling problems of the opamps are getting even more severe. It should be

emphasized that the E-type SC biquadratic filter without double-sampling operation would still be good enough in terms of settling of opamps. Considering the original E-type SC biquad architecture (schematic draws in black colour), opamp A_2 integrates the charge from capacitor C_A only during ϕ_1, where opamp A_2 settles. On the other hand, the output of the opamp A_2 is fed back to the opamp A_1 only during ϕ_2. Hence, the two opamps will settle in different clock phases and thus their settlings are not affecting each other.

In fact, the solution for the settling problems of the opamps can be readily observed from this architecture as well. Considering the non-inverting SC integrator formed by opamp A_2 and integration capacitor C_B, the input sampling capacitors C_A always sample the output of opamp A_1 in one clock phase, while passing the sampled data to opamp A_2 in next clock phase. Consequently, the settling of opamp A_2 is independent to the settling of opamp A_1.

Though it is readily motivating enough to adopt only non-inverting SC integrators to realize a double-sampled SC biquadratic filter, connecting two non-inverting SC integrators in a loop would create positive feedback configuration, which is unstable. This also explains the reason why most of the SC architectures adopt both non-inverting and inverting SC integrators. In next section, the issues on achieving stable operation and generic coefficients of the proposed double-sampled SC biquadratic filter based on non-inverting SC integrators are addressed.

Lastly, when cascading several stages of SC circuits to form a high-order SC system, the input sampling branch formed by C_G should be employed to isolate the cascaded stages. Besides, it should be careful when applying double-sampling technique to conventional SC circuits, as there also exist some exceptional cases that the employment of double-sampling technique would change the transfer function of the original circuit.

3.4 Proposed Fast-Settling Double-Sampled Generic SC Biquadratic Filter

Figure 3.4 shows the proposed fast-settling double-sampled SC biquadratic filter architecture [CHE 02b, CHE 02b]. The corresponding minimum switch configuration can be easily obtained by combining those switches with same function. Equation 3.1 describes the transfer function of the proposed SC filter.

$$H(z)=\frac{V_{out}(z)}{V_{in}(z)}=-\frac{DI+(AG-DI-DJ)z^{-1}+(DJ-AH)z^{-2}}{BD+(DF+BE-2BD)z^{-1}+(BD+FE+AC-FD-BE)z^{-2}} \quad \text{(Eq. 3.1)}$$

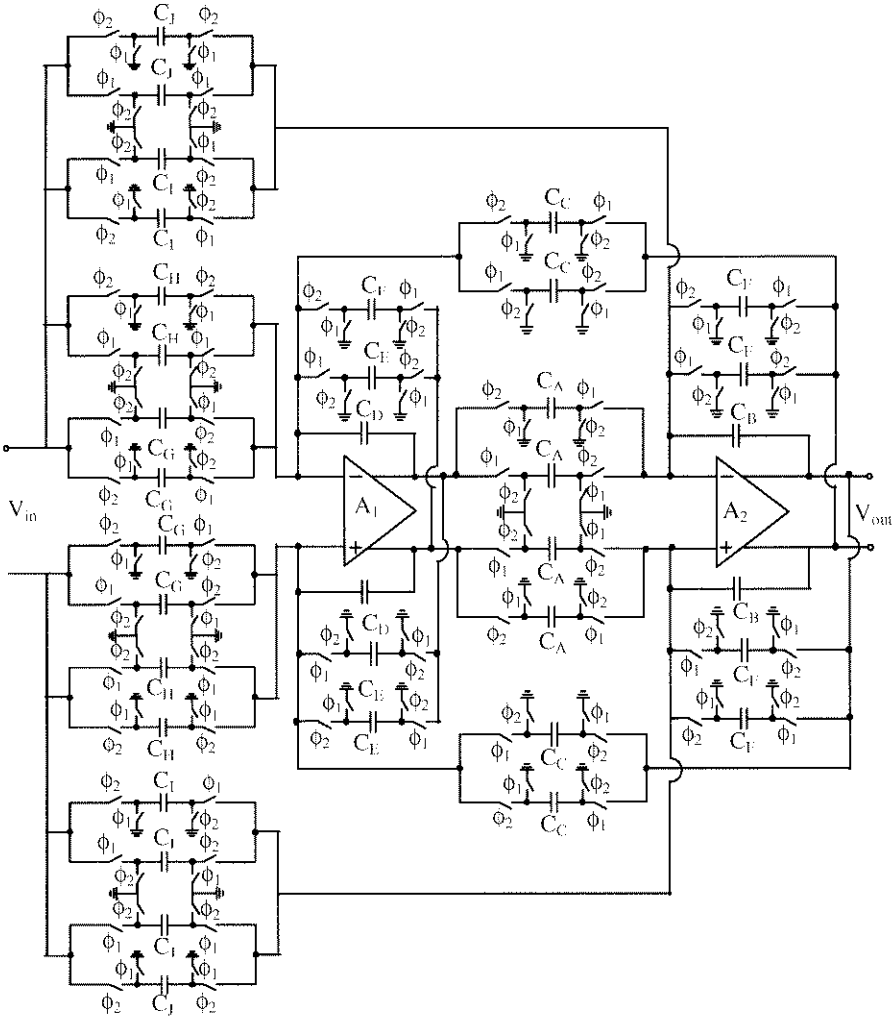


Figure 3.4 Generic Fast-Settling Double-Sampling SC Biquadratic Filter

By operating in a double-sampling manner, and the unity-gain-frequency requirement of the opamps is reduced by 50%, compared with conventional SC biquadratic filter [FLE 79]. Moreover, unlike the double-sampled SC biquadratic filter in [NAG 97], the proposed architecture employs only non-inverting delay SC integrators for the realization of the core of the filter such that there is no direct feedback in the architecture. As a result, the two opamps are decoupled from each other to achieve independent and fast settling. Besides, the use of non-inventing delay SC integrators is also immune to parasitic effects [GRE 86]. A fully-differential architecture not only helps reject common-mode noise, but also provide a free sign inversion

for switched capacitors C_E, C_F and C_C to achieve for stable operation while maintaining a generic transfer function.

3.5 Proposed Half-Delay-SC-Integrator-Based Generic SC Biquadratic Filter

Figure 3.5 shows the proposed generic SC biquadratic filter.

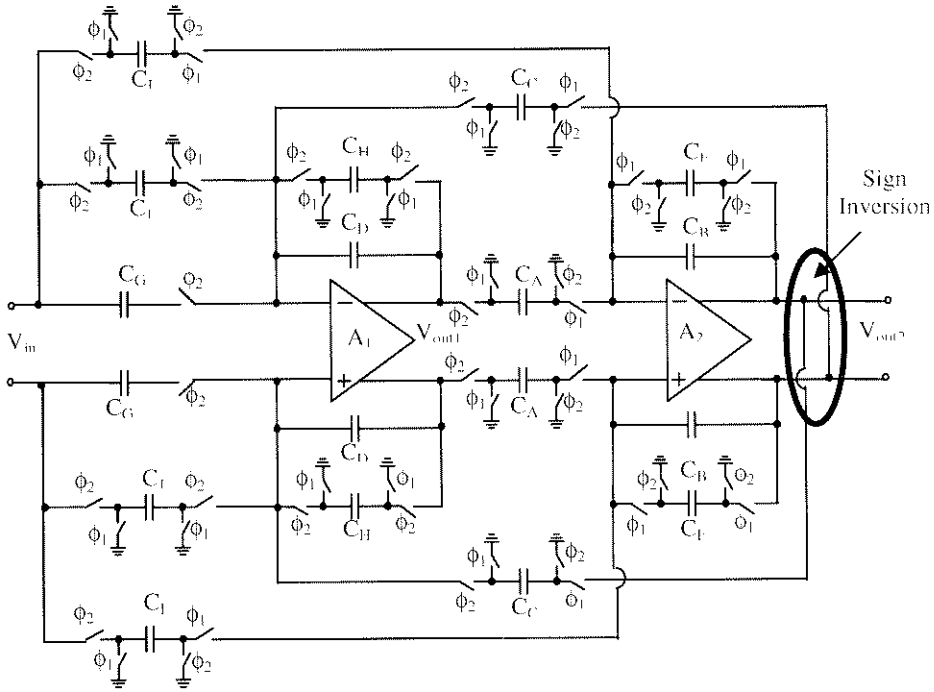


Figure 3.5 Generic Half-Delay-SC-Integrator-Based SC Biquadratic Filter

The core of the proposed filter consists of two half-delay non-inverting SC integrators connected in closed-loop form to work as a second-order resonator. To make the overall architecture in a negative feedback configuration for stable operation, sign inversion technique [INO 86] is applied. A free sign inversion can be obtained by connecting the switched capacitors C_C inversely at the differential outputs of opamp A_2.

An important criterion of the design of the proposed architecture is on the adoption of only two opamps, which can be turned off after their integration phases to save power. With this consideration, the switched capacitors C_H and C_F, which perform the damping factors of the filter, are connected respectively across the opamps A_1 and A_2 during their integration phases ϕ_2

and ϕ_1. On the other hand, the three switched capacitors (C_G, C_J) and C_I which enable the proposed filter with transfer function having a generic nominator, sample the input signal and pass the sampled data respectively to the opamps A_1 and A_2 also during only their integration phases ϕ_2 and ϕ_1.

In general, the input signal of SC filter is continuous unless a sample-and-hold circuit is employed in front of the filter [GRE 86]. For general applications, the filter is designed to sample the input signal only during ϕ_2 but not at both clock phases. It should be emphasized that the sampling of the input signal at both ϕ_1 and ϕ_2 clock phases would only insert in the nominator of the transfer function some half-delay coefficients, which are not useful for designing of real SC filters.

To obtain the transfer function of the proposed biquadratic filter, time-domain analysis [KI 95] is performed. The opamp, capacitors and switches are considered perfect. Table 3.1 summarizes the charge transfer occurs at all capacitors.

Table 3.1 Timing Diagram Showing the Charge Transferring that Occurs at All Capacitors

$\phi_1 \rightarrow \phi_2$		$\phi_2 \rightarrow \phi_1$	
$\phi_1 = 1.\left[(n-1).\left(n-\frac{1}{2}\right)\right]$	$\phi_2 = 1.\left[\left(n-\frac{1}{2}\right).(n)\right]$	$\phi_1 = 1.\left[(n).\left(n+\frac{1}{2}\right)\right]$	Cap
$V_A(n-1)=0$	$V_A\left(n-\frac{1}{2}\right)=V_{out1}\left(n-\frac{1}{2}\right)$	$V_A(n)=0$	C_A
$V_B(n-1)=-V_{out2}(n-1)$	$V_B\left(n-\frac{1}{2}\right)=-V_{out2}\left(n-\frac{1}{2}\right)$	$V_B(n)=-V_{out2}(n)$	C_B
No change →			
$V_C(n-1)=+V_{out2}(n-1)$	$V_C\left(n-\frac{1}{2}\right)=0$	$V_C(n)=+V_{out2}(n)$	C_C
$V_D(n-1)=-V_{out1}(n-1)$	$V_D\left(n-\frac{1}{2}\right)=-V_{out1}\left(n-\frac{1}{2}\right)$	$V_D(n)=-V_{out1}(n)$	C_D
	No change →		
$V_E(n-1)=-V_{out2}(n-1)$	$V_E\left(n-\frac{1}{2}\right)=0$	$V_E(n)=-V_{out2}(n)$	C_E
$V_G(n-1)=V_{IN}\left(n-\frac{3}{2}\right)$	$V_G\left(n-\frac{1}{2}\right)=V_{IN}\left(n-\frac{1}{2}\right)$	$V_G(n-1)=V_{IN}\left(n-\frac{1}{2}\right)$	C_G
$V_H(n-1)=0$	$V_H\left(n-\frac{1}{2}\right)=-V_{out1}\left(n-\frac{1}{2}\right)$	$V_H(n)=0$	C_H
$V_I(n-1)=0$	$V_I\left(n-\frac{1}{2}\right)=V_{IN}\left(n-\frac{1}{2}\right)$	$V_I(n)=0$	C_I
$V_J(n-1)=0$	$V_J\left(n-\frac{1}{2}\right)=V_{IN}\left(n-\frac{1}{2}\right)$	$V_J(n)=0$	C_J

Notice that: $V_{out2}(n-1)=V_{out2}\left(n-\frac{1}{2}\right)$

$V_{out1}(n)=V_{out1}\left(n-\frac{1}{2}\right)$

By Kirchhoff Charge Law, during $\phi_1 \rightarrow \phi_2$ transition, i.e. from time (n-1) to (n-1/2), the sum of the change in charge of capacitors C_G (ΔQ_G) and C_J (ΔQ_J) is equal to that of capacitor C_H (ΔQ_H), C_D (ΔQ_D) and C_C (ΔQ_C).

$$i.e.\ \Delta Q_G + \Delta Q_J = \Delta Q_H + \Delta Q_D + \Delta Q_C ,$$

$$\Rightarrow C_G\left[V_{IN}\left(n-\tfrac{1}{2}\right)-V_{IN}\left(n-\tfrac{3}{2}\right)\right]+C_J\left[V_{IN}\left(n-\tfrac{1}{2}\right)-0\right]$$
$$= C_H\left[-V_{out1}\left(n-\tfrac{1}{2}\right)-0\right]+C_D\left[-V_{out1}\left(n-\tfrac{1}{2}\right)+V_{out1}(n-1)\right]$$
$$+ C_C\left[0-V_{out2}\left(n-\tfrac{1}{2}\right)\right]$$

$$\xrightarrow{Z\text{-}Transformation}$$

$$\Rightarrow C_G\left(z^{-1/2}-z^{-3/2}\right)V_{IN}(z)+C_J V_{IN}(z)$$
$$= -C_H z^{-1/2}V_{out1}(z)+C_D\left(-z^{-1/2}+z^{-3/2}\right)V_{out1}(z)$$
$$+ C_C z^{-1/2}V_{out2}(z)$$

$$\Rightarrow \left[C_G\left(1-z^{-1}\right)+C_J\right]V_{IN}(z)$$
$$= -\left[C_H + C_D\left(1-z^{-1}\right)\right]V_{out1}(z)-C_C V_{out2}(z) \qquad \text{(Eq. 3.2)}$$

Consider during the $\phi_1 \rightarrow \phi_2$ transition, i.e. from time (n-1/2) to (n), the sum of the change in charge of capacitors C_A (ΔQ_A) and C_I (ΔQ_I) is equal to that of capacitor C_B (ΔQ_B) and C_F (ΔQ_F).

$$i.e.\ \Delta Q_A + \Delta Q_I = \Delta Q_B + \Delta Q_F ,$$

$$\Rightarrow C_A\left[0-V_{out1}\left(n-\tfrac{1}{2}\right)\right]+C_I\left[0-V_{IN}\left(n-\tfrac{1}{2}\right)\right]$$
$$= C_B\left[-V_{out2}(n)-V_{out2}\left(n-\tfrac{1}{2}\right)\right]+C_F\left[-V_{out2}(n)-0\right]$$

$$\xrightarrow{Z\text{-}Transformation}$$

$$\Rightarrow -C_A z^{-1/2}V_{out1}(z)-C_I z^{-1/2}V_{IN}(z)$$
$$= C_B\left(-z^{1/2}+z^{-1/2}\right)V_{out2}(z)-C_F z^{1/2}V_{out2}(z)$$

$$\Rightarrow C_A z^{-1}V_{out1}(z)+C_I z^{-1}V_{IN}(z)=\left[C_F + C_B\left(1-z^{-1}\right)\right]V_{out2}(z) \qquad \text{(Eq. 3.3)}$$

Substituting Equation 3.3 into Equation 3.2 to equate $V_{out1}(z)/V_{IN}(z)$:

$$\Rightarrow C_A z^{-1} V_{out1}(z) + C_I z^{-1} V_{IN}(z)$$
$$= -\left[C_F + C_B(1 - z^{-1})\right]\left[\frac{\left[C_H + C_D(1 - z^{-1})\right] V_{out1}(z) - \left[C_J + C_G(1 - z^{-1})\right] V_{IN}(z)}{C_C}\right]$$

$$\frac{V_{out1}(z)}{V_{IN}(z)} = -\frac{(C_B + C_F)(C_G + C_J) - [C_B(C_G + C_J) + C_G(C_B + C_F) - C_J C_C]z^{-1} + C_B C_G z^{-2}}{(C_H + C_D)(C_B + C_F) - [C_B(C_H + C_D) + C_D(C_B + C_F) - C_A C_C]z^{-1} + C_B C_D z^{-2}}$$

---------- (Eq. 3.4)

Substituting Equation 3.2 into Equation 3.3 to equate $V_{out2}(z)/V_{IN}(z)$:

$$\Rightarrow \left[C_J + C_G(1 - z^{-1})\right] V_{IN}(z)$$
$$= -\left[C_H + C_D(1 - z^{-1})\right]\left[\frac{\left[C_F + C_B(1 - z^{-1})\right] V_{out2}(z) - C_I z^{-1} V_{IN}(z)}{C_A z^{-1}}\right] - C_C V_{out2}(z)$$

$$\frac{V_{out2}(z)}{V_{IN}(z)} = \frac{[C_I(C_H + C_D) - C_A(C_G + C_J)]z^{-1} - (C_D C_J + C_A C_G)z^{-2}}{(C_H + C_D)(C_B + C_F) - [C_B(C_H + C_D) + C_D(C_B + C_F) - C_A C_C]z^{-1} + C_B C_D z^{-2}}$$

---------- (Eq. 3.5)

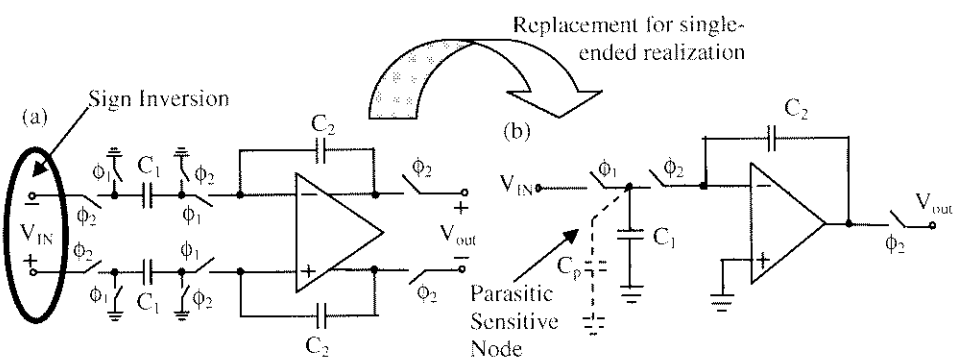
Equations 3.4 and 3.5 describe the transfer functions of the proposed biquadratic filter with output taken at opamp A_2 and A_1 respectively. As for most of the conventional SC biquadratic filters, equations 3.4 and 3.5 have same denominator, which determine the location of the poles of the filter. The main difference between the two transfer functions is that equation 3.3 does not contain the integer term (non z-term) in the nominator, which positions the zeros of the filter. Nevertheless, the lack of the integer term in the nominator would only affect the realization of all-pass function [ANA 95] with $V_{out2}(z)$ taken as the output of the proposed filter.

In a fully-differential realization, the input switched capacitors C_G, C_I and C_J can be inversely connected to achieve for negative coefficients in the nominator of the transfer function to facilitate the realization of the zeros. Sign inversion of other switched capacitors is limited, however, by stability concern. Certainly, the integrating capacitors C_D and C_B must be connected respectively across the opamps A_1 and A_2 in negative feedback configurations for stable operation. The switched capacitors C_H and C_F are, however, conditionally stable to be inversely connected between the differential path provided that $C_H < C_D$ and $C_F < C_B$ such that the overall

feedback across each of the opamps is still negative at any time instance. Lastly, either but not both of the switched capacitors C_A and C_C must be inversely connected to maintain a negative feedback of the whole loop as indicated in Fig. 3.5.

Since both of the switched capacitors C_H and C_F provide the damping factors of the filter, either one of them is necessary to be employed. It is interesting to point out that switched capacitor C_H does not affect the placement of the zeros in Equation 3.5 while in Equation 3.4, it affects the placement of both the zeros and poles. Therefore, it is more desirable in terms of the sensitivity to variations of elements to employ switched capacitor C_F instead of C_H in Equation 3.4. Similarly, since the switched capacitor C_F also affects the placement of both the zeros and poles in Equation 3.5, switched-capacitor C_H should be employed instead if output V_{out2} is taken.

The proposed filter is generic and parasitic-insensitive in a fully-differential realization. However, for single-ended implementation, free sign inversion cannot be obtained. As a result, in order to keep the stability of the loop, parasitic-sensitive switched-capacitor branch has to be employed to replace either but not both the switched capacitor C_A or C_C as illustrated in Fig. 3.6.



$$H_{Ideal}(z) = \frac{V_{out}(z)}{V_{IN}(z)} = -\frac{C_1 z^{-1/2}}{C_2\left(1 - z^{-1}\right)}$$

Figure 3.6 (a) Parasitic-Insensitive Non-Inverting Integrator with Sign Inversion; (b) Parasitic-Sensitive Inverting Integrator

Both of the integrators require the opamps to be active only during their integration phases and thus maintaining the power efficiency of the architecture. Nevertheless, the single-ended architecture is parasitic sensitive and suffers from noise and interference from the operating environment.

3.6 Proposed Half-Delay-SC-Integrator-Based SC Ladder Filter

SC ladder filter [GRE 86] has been widely employed for realizing high-order filter transfer function. Though first- and second-order SC filters, in principle, can be cascaded to realize any high-order transfer function. In practice, however, the resulting circuit is often very sensitive to process variations for high order and selective filters. The reason is that for such filters, the response of each of the cascaded sections, which realizes high-Q poles, is very sensitive to element variations. The SC ladder filter, instead of cascading first- and second-order SC filters, achieves high-order transfer function based on simulating the low-sensitivity response of a doubly terminated LCR circuit prototype with equivalent SC circuits. Hence, the resulting filter is less sensitive to process variations than it is achieved by cascading low-order SC sections. Figure 3.7 shows the schematic of a 5th-order Chebyshev LCR prototype circuit. Since the characteristics of the lowpass LCR prototype can be easily obtained from most of the filter data books [NIE 89], the derivation of the SC ladder filter.

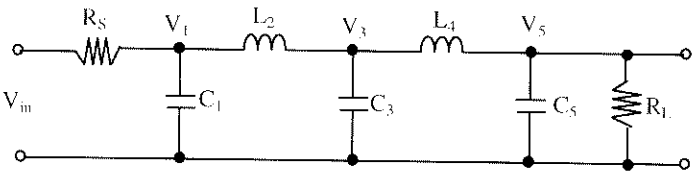


Figure 3.7 A 5th-Order LCR Filter Prototype Circuit

The state-space equations of the 5th-order LCR prototype circuit can be written as follows:

$$-V_1 = -\frac{1}{sC_1}\left[\frac{V_{in}-V_1}{R_S} - I_2\right]$$

$$-I_2 = \frac{-1}{sL_2}(V_1 - V_3)$$

$$V_3 = \frac{-1}{sC_3}[-I_2 + I_4]$$

$$I_4 = \frac{1}{sL_4}(V_3 - V_5)$$

$$-V_1 = -\frac{1}{sC_5}\left[\frac{-V_5}{R_L} + I_4\right]$$

The state-space equations can also be presented in a block diagram as shown in Fig. 3.8.

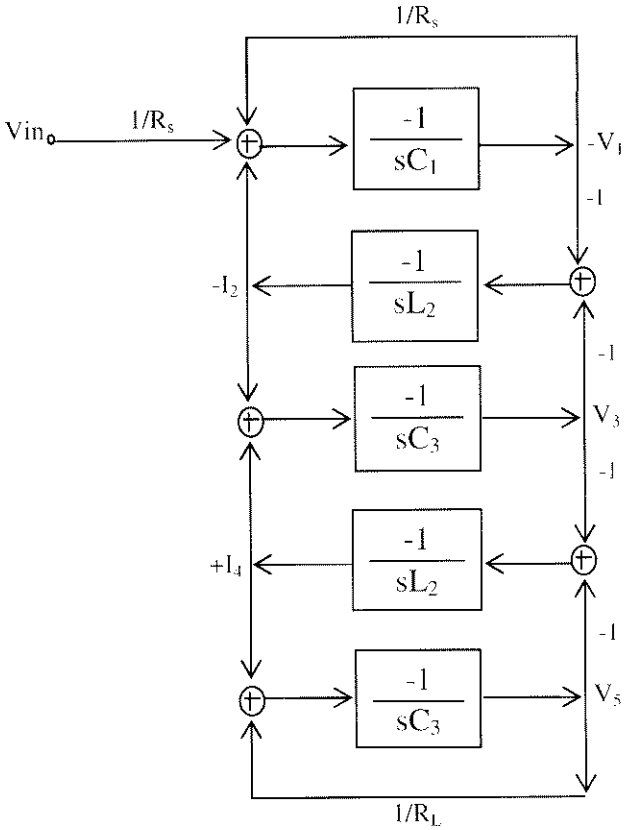


Figure 3.8 Block Diagram Describing the State-Space Equations

It can be observed that all the blocks represent the transfer function of an integrator in the continuous-time domain (s-domain). By performing the s-to-z transformation, the corresponding z-domain transfer function of the block diagram is obtained. Among all the s-to-z transformations, LDI-transformation [GRE 86] provides an accurate and simple realization of the block diagram. This is because the LDI-transformed integrator that realized with SC circuit is exactly same as a continuous time integrator. The resulting implementation of the SC ladder filter is shown in Fig. 3.9.

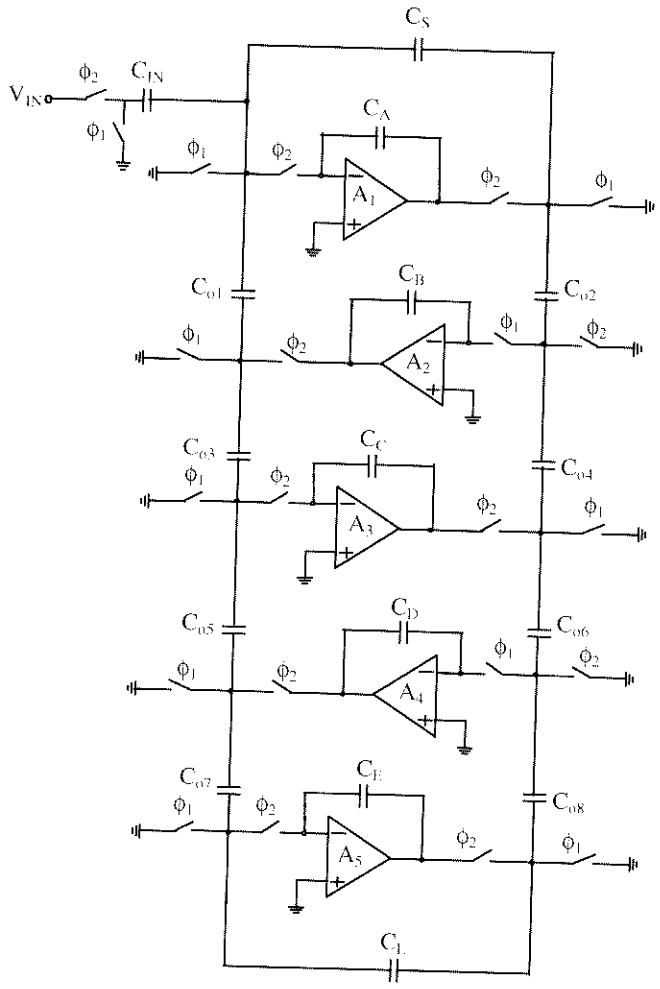


Figure 3.9 LDI-Transformed Switched-Capacitor Lowpass Ladder Filter

The resulting lowpass ladder filter shares the low-sensitivity properties of the LCR prototype filter. Besides, the filter is constructed using only parasitic-insensitive integrators thus further improving the immunity to process variations. The detailed design equations of the ladder filter are provided in Appendix C of this dissertation.

It can be observed from Fig. 3.9 that opamps A_1, A_3 and A_5 are employed to realize non-delay inverting integrators. All of these integrators perform integration only during ϕ_2. Therefore, during ϕ_1, the opamps A_1, A_3 and A_5 are idle and can be turned off to save power. However, the opamps A_2 and A_4 are realizing non-inverting integrators that require these opamps to be active

at all time. Fig. 3.10(a) extracts the opamps A_2 and A_3, which form a SC gyrator.

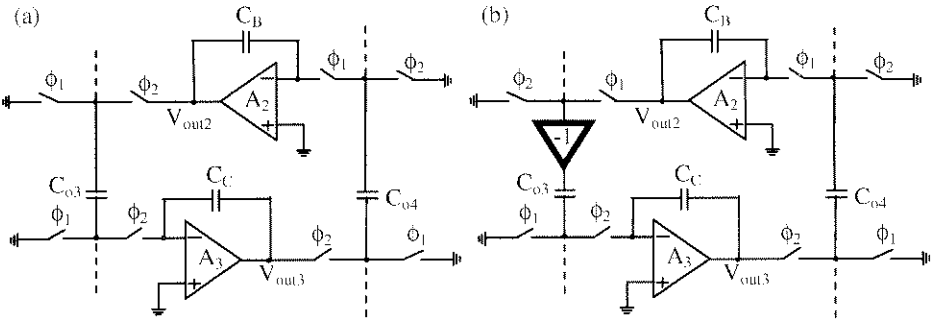


Figure 3.10 (a) Original SC Gyrator in the Lowpass Ladder Filter; (b) Modified SC Gyrator Using Half-Delay Non-Inverting Integrators

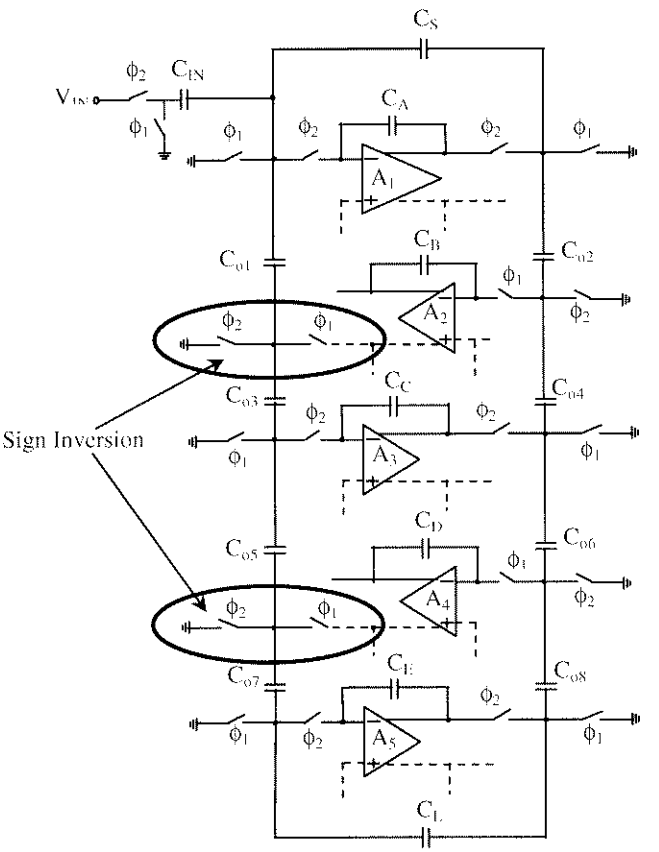


Figure 3.11 Proposed Half-Delay-SC-Integrator-Based Lowpass Ladder Filter

In order to realize the SC lowpass ladder filter using only half-delay non-inverting integrators to achieve for the lowest possible power consumption, some modifications are necessary. In fact, by interchanging the clock phases of the switches that connect at outputs of opamp A_2 and inserting a sign inversion, an equivalent SC gyrator can be realized using only half-delay non-inverting SC integrators as shown in Fig. 3.10(b). The sign inversion of the output signal of the opamps can be freely obtained from a fully-differential structure, which also helps reject common-mode noise and reduces clock-feedthrough noise. Fig. 3.11 shows the proposed fully-differential half-delay-SC-integrator-based SC lowpass ladder filter.

The proposed SC lowpass ladder filter, when implemented with switched-opamp technique, could save up to 50 % power consumption compared with the conventional realization. This is due to the adoption of half-delay non-inverting SC integrators as the basic building block, which allow the opamps to be turned off after their integration phases.

3.7 Proposed Half-Delay-SC-Integrator-Based SC Lowpass ΣΔ Modulator with Noise-Shaping Extension

Fig. 3.12 shows the linear model of the proposed 3rd-order lowpass ΣΔ modulator, which consists of three half-delay non-inverting integrators, a 1-bit Digital-to-Analog Converter (DAC) and a quantizer. Equation 3.6 describes the ideal transfer characteristic of the ΣΔ modulator.

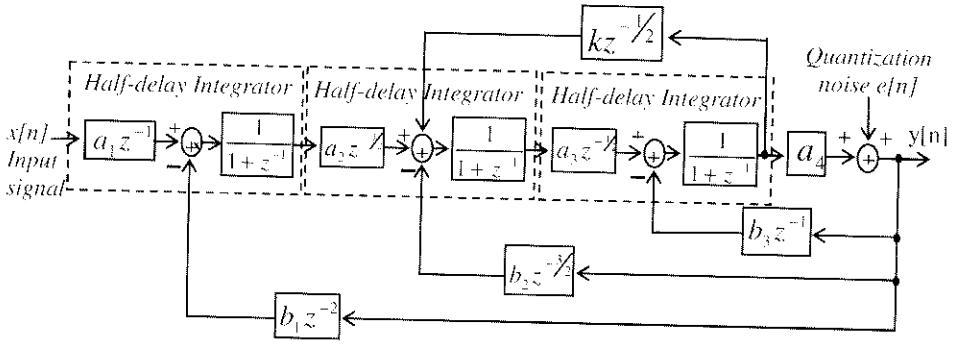


Figure 3.12 Linear Model of the Half-Delay-Integrator-Based Lowpass ΣΔ Modulator with Noise-Shaping Extension

$$Y(z) = z^{-2}X(z) + \left(1 - z^{-1}\right)\left[1 - (2 - a_3 k)z^{-1} + z^{-2}\right]E(z) \qquad \text{(Eq. 3.6)}$$

The first integrator suppresses the quantization noise at the DC, while the second and the third integrators can be configured as a resonator to suppress the quantization noise at low-frequency regions. The noise-shaping region is extended to enhance the resolution without increasing the over-sampling-ratio (OSR), which in turn reduces the power consumption. The position of the resonator is determined by the parameter a_3k in Equation 3.6. Specifically, by setting the parameter a_3k to be zero, the architecture returns to a conventional 3[rd]-order lowpass topology [AZI 96, COB 00], which creates a 3[rd]-order notch to suppress the quantization noise at the DC. The design equations to apply the noise-shaping extension technique are derived as follows:

The designed center frequency ($\omega_o = 2\pi f_o$) of the resonator is swapped into the z-domain by LDI-transformation (GRE 86):

$$\omega_a = \frac{1}{T}\sin(\omega_o T)$$

$$For\ \omega_o << \omega_s \Rightarrow \omega T << 1$$

$$\Rightarrow \omega_a \approx \omega_o$$

$$\Rightarrow f_a \approx f_o$$

where f_a is the center frequency of the resonator in the z-domain. The transfer function of the resonator is given in the z-domain by [Appendix B]:

$$H(z) = \frac{N(s)}{1-(2-\alpha-\beta)z^{-1}+(1-\beta)z^{-2}}$$

$$For\ a\ resonator,\ Q = \infty$$

$$\therefore \alpha = \frac{4}{\left(\frac{2f_s}{2\pi f_a}\right)^2 + \frac{\left(\frac{2f_s}{2\pi f_a}\right)}{Q} + 1} \approx \left(\frac{2\pi f_a}{f_s}\right)^2$$

$$\beta = 0$$

Hence, α represents the relationship between the center frequency f_o of the resonator and the sampling frequency f_s of the system.

For a 1-bit quantizer having a zero mean error e[n], its variance σ_e^2 (power) is given by:

$$\sigma_e^2 = \frac{1}{\Delta}\int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} e^2 de = \frac{\Delta^2}{12}$$

When a quantized signal is sampled at frequency $f_s = 1/T$, all of its power folds into the frequency band $0 \le f < f_s$. Assume the quantizer has a white noise spectral [A.PZI 96], the spectral density of the sampled noise is given by:

$$E(f) = \sqrt{\frac{\sigma_e^2}{f_s/2}} = \sigma_e\sqrt{\frac{2}{f_s}}$$

The noise spectral density of the quantizer is shaped by the proposed lowpass ΣΔ modulator:

$$E(z)\left(1-z^{-1}\right)\left[1-(2-\alpha)z^{-1}+z^{-2}\right]$$

Hence, the in-band (interested bandwidth: $f_{BW1} \le f \le f_{BW2}$) quantization noise power of the ΣΔ modulator can be calculated as follows:

$$N(f) = \int_{f_{BW1}}^{f_{BW2}} E^2(f)\left|1-z^{-1}\right|^2\left|1-(2-\alpha)z^{-1}+z^{-2}\right|^2 df$$

Substituting $z = e^{j\theta} = \cos\theta - j\sin\theta$, where $\theta = 2\pi f/f_s$,

$$\begin{aligned}\left|1-z^{-1}\right|^2 &= \left|1-\cos\theta+j\sin\theta\right|^2 \\ &= (1-\cos\theta)^2+(\sin\theta)^2 \\ &= 2-2\cos\theta \\ &= 4\sin^2\left(\frac{\theta}{2}\right) \approx \theta^2\end{aligned}$$

$$
\begin{aligned}
\left|1-(2-\alpha)z^{-1}+z^{-2}\right|^2 &= \left|1-(2-\alpha)(\cos\theta - j\sin\theta)+(\cos(2\theta)-j\sin(2\theta))\right|^2 \\
&= \left[1-(2-\alpha)\cos\theta+\cos(2\theta)\right]^2 + \left[(2-\alpha)(\sin\theta)-\sin(2\theta)\right]^2 \\
&= \left[1-(2-\alpha)\cos\theta\right]^2 + 2\left[1-(2-\alpha)\cos\theta\right]\cos(2\theta)+\cos^2(2\theta) \\
&\quad + (2-\alpha)^2\sin^2\theta - 2(2-\alpha)\sin\theta\sin(2\theta)+\sin^2(2\theta) \\
&= \left[1-2(2-\alpha)\cos\theta+(2-\alpha)^2\cos^2\theta\right]+2\left[\cos(2\theta)-(2-\alpha)\cos\theta\cos(2\theta)\right] \\
&\quad + \cos^2(2\theta)+(2-\alpha)^2\sin^2\theta - 2(2-\alpha)\sin\theta\sin(2\theta)+\sin^2(2\theta) \\
&= 2-2(2-\alpha)\cos\theta+(2-\alpha)^2+2\cos(2\theta) \\
&\quad - \left[2(2-\alpha)\cos\theta\cos(2\theta)+2(2-\alpha)\sin\theta\sin(2\theta)\right] \\
&= 2(1+\cos(2\theta))-2(2-\alpha)\cos\theta+(2-\alpha)^2-2(2-\alpha)\cos(2\theta-\theta) \\
&= (2-\alpha)^2-4(2-\alpha)\cos\theta+4\cos^2\theta \\
&= (2-\alpha-2\cos\theta)^2 \\
&= \left(4\sin^2\left(\frac{\theta}{2}\right)-\alpha\right)^2 \\
&\approx (\theta^2-\alpha)^2
\end{aligned}
$$

$$
\begin{aligned}
\Rightarrow N(f) &= \int_{f_{BW1}}^{f_{BW2}} E^2(f)(\theta^2)(\theta^2-\alpha)^2\,df \\
&= \int_{f_{BW1}}^{f_{BW2}} \left(\frac{\sigma_e^2}{f_s/2}\right)\left(\frac{2\pi f}{f_s}\right)^2\left(\left(\frac{2\pi f}{f_s}\right)^2-\alpha\right)^2 df \\
&= \int_{f_{BW1}}^{f_{BW2}} \left(\frac{\sigma_e^2}{f_s/2}\right)\left(\frac{2\pi f}{f_s}\right)^2\left(\left(\frac{2\pi f}{f_s}\right)^2-\left(\frac{2\pi f_a}{f_s}\right)^2\right)^2 df \\
&= \left(\frac{128\pi^6\sigma_e^2}{{f_s}^7}\right)\int_{f_{BW1}}^{f_{BW2}} (f)^2\left(f^2-{f_a}^2\right)^2 df \\
&= \left(\frac{128\pi^6\sigma_e^2}{{f_s}^7}\right)\left[\frac{1}{7}f^7-\frac{2}{5}{f_a}^2f^5+\frac{1}{3}{f_a}^4f^3\right]_{f_{BW1}}^{f_{BW2}} \\
&= \left(\frac{128\pi^6\sigma_e^2}{{f_s}^7}\right)\left[\left(\frac{1}{7}{f_{BW2}}^7-\frac{2}{5}{f_a}^2{f_{BW2}}^5+\frac{1}{3}{f_a}^4{f_{BW2}}^3\right)\right. \\
&\quad \left.-\left(\frac{1}{7}{f_{BW1}}^7-\frac{2}{5}{f_a}^2{f_{BW1}}^5+\frac{1}{3}{f_a}^4{f_{BW1}}^3\right)\right] \qquad \text{(Eq. 3.7)}
\end{aligned}
$$

Equation 3.7 describes the total noise power of the proposed ΣΔ modulator. If noise-shaping extension technique is not employed, i.e. $f_a = 0$, the proposed ΣΔ modulator works as same as a conventional 3rd-order lowpass ΣΔ modulator, which has a total noise power given by Equation 3.8:

$$\Rightarrow N_o(f) = \int_{f_{BW1}}^{f_{BW2}} E^2(f)(\theta)^6 df$$

$$= \int_{f_{BW1}}^{f_{BW2}} \left(\frac{\sigma_e^2}{f_s/2}\right)\left(\frac{2\pi f}{f_s}\right)^6 df$$

$$= \left(\frac{128\pi^6\sigma_e^2}{{f_s}^7}\right)\int_{f_{BW1}}^{f_{BW2}} (f)^6 df$$

$$= \left(\frac{128\pi^6\sigma_e^2}{{f_s}^7}\right)\left[\frac{1}{7}f^7\right]_{f_{BW1}}^{f_{BW2}}$$

$$= \left(\frac{128\pi^6\sigma_e^2}{{f_s}^7}\right)\left(\frac{1}{7}{f_{BW2}}^7 - \frac{1}{7}{f_{BW1}}^7\right) \qquad \text{(Eq. 3.8)}$$

The performance of the proposed ΣΔ modulator and the conventional design can be compared by writing the ratio of their noise power as a function of the center frequency f_o of the resonator in the proposed ΣΔ modulator:

$$\frac{N_o(f)}{N(f)}$$

$$= \frac{\frac{1}{7}\left({f_{BW2}}^7 - {f_{BW1}}^7\right)}{\left(\frac{1}{7}{f_{BW2}}^7 - \frac{2}{5}{f_a}^2{f_{BW2}}^5 + \frac{1}{3}{f_a}^4{f_{BW2}}^3\right) - \left(\frac{1}{7}{f_{BW1}}^7 - \frac{2}{5}{f_a}^2{f_{BW1}}^5 + \frac{1}{3}{f_a}^4{f_{BW1}}^3\right)}$$

$$= \frac{{f_{BW2}}^7 - {f_{BW1}}^7}{\left({f_{BW2}}^7 - \frac{14}{5}{f_a}^2{f_{BW2}}^5 + \frac{7}{3}{f_a}^4{f_{BW2}}^3\right) - \left({f_{BW1}}^7 - \frac{14}{5}{f_a}^2{f_{BW1}}^5 + \frac{7}{3}{f_a}^4{f_{BW1}}^3\right)}$$

---------- (Eq. 3.9)

Consider both ΣΔ modulators have an interested bandwidth of $0 < f < f_{BW}$ (i.e. $f_{BW1} = 0$, $f_{BW2} = f_{BW}$), Equation 3.9 is simplified as shown in Equation 3.10. The result is plotted as shown in Fig. 13.

$$\frac{N_o(f)}{N(f)} = \frac{\frac{1}{7} f_{BW2}^{\ 7}}{\frac{1}{7} f_{BW2}^{\ 7} - \frac{2}{5} f_a^{\ 2} f_{BW2}^{\ 5} + \frac{1}{3} f_a^{\ 4} f_{BW2}^{\ 3}} = \frac{1}{1 - \frac{14}{5}\frac{f_a^{\ 2}}{f_{BW2}^{\ 2}} + \frac{7}{3}\frac{f_a^{\ 4}}{f_{BW2}^{\ 4}}} \qquad \text{(Eq. 3.10)}$$

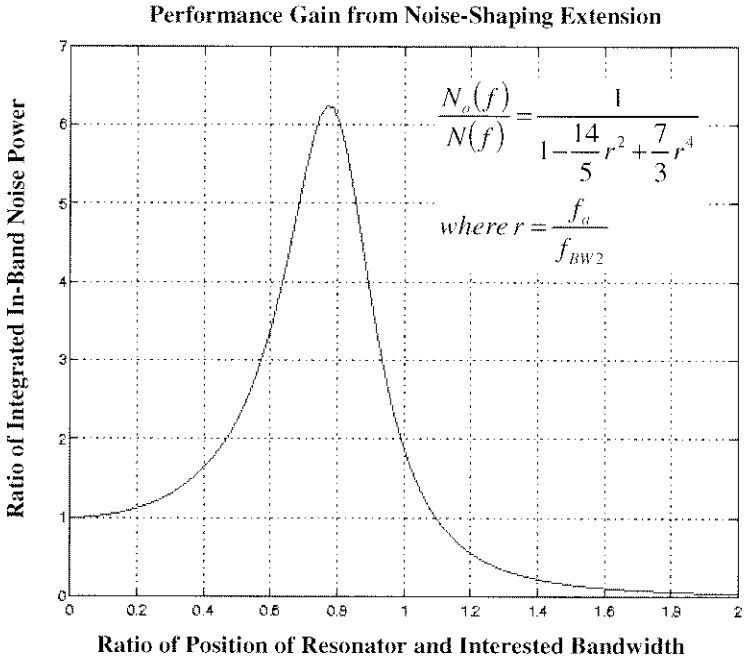


Figure 3.13 Plots of Noise Power Reduction with Optimal Placement of Resonator

The peak value of $N_o(f)/N(f)$ is 6.25, which corresponds to a noise reduction of 16 dB when the resonator is positioned at 0.76 f_{BW}. The proposed noise-shaping extension technique thus minimizing the quantization noise at a given over-sampling-ratio. As a result, without dissipating extra power, the proposed ΣΔ modulator achieves much better signal-to-noise-ratio than the

conventional realization. It should be emphasized that when the interested bandwidth does not include the DC (i.e. $f_{BW1} \neq 0$), the effectiveness of the proposed noise shaping extension technique would be even higher since the conventional lowpass ΣΔ modulator is only most efficient in noise suppression at frequency near DC. Nevertheless, when f_{BW1} is too high, lowpass ΣΔ modulator, with or without noise-shaping extension, may not be applicable unless a higher over-sampling-ratio is employed. A bandpass ΣΔ modulator [AZI 96] or a pipelined analog-to-digital converter [ABO 99] may be applied instead. Lastly, if f_{BW1} is not zero (does not cover the DC), Equation 3.9 can be applied to find the optimal placement of the resonator. Fig. 3.14 shows the schematic of a fully-differential realization of the proposed 3rd-order lowpass ΣΔ modulator.

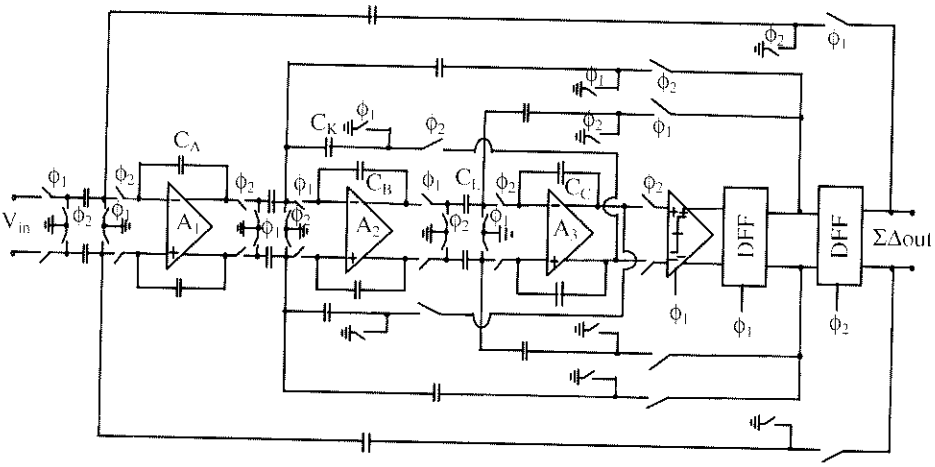


Figure 3.14 SC Implementation of the Half-Delay-Integrator-Based Lowpass ΣΔ Modulator with Noise-Shaping Extension

Opamps A_1 realizes the first integrator of the modulator while the opamps A_2 and A_3 can be configured to implement the resonator to achieve for the proposed noise-shaping extension. Equation 3.11 describes the design equation of the proposed ΣΔ modulator.

$$Y(z) = z^{-2}X(z) + (1 - z^{-1})\left[1 - \left(2 - \frac{C_K C_L}{C_B C_C}\right)z^{-1} + z^{-2}\right]E(z) \qquad \text{(Eq. 3.11)}$$

The advantage of using half-delay integrators for the implementation is that the opamps are required to be active only during their integration phases. As

a result, these opamps can be turned off to save power or time-shared for other circuits after their integration phases. The proposed ΣΔ modulator works as a conventional design when switched capacitor C_K is ignored.

3.8 Conclusion

To improve the performance of switched-opamp circuits, novel SC architectures are proposed. In term of operation speed, a fast-settling double-sampled SC architecture has been proposed and successfully employed to realize a 10.7-MHz bandpass ΣΔ modulator [CHE 02b] in a single 1-V supply as will be discussed in Chapter 6. In term of reducing power consumption, the development of a family of half-delay-SC-integrator-based SC filters and ΣΔ modulator reduces the required power consumption by 50 % compared with conventional realization. Besides, a noise-shaping extension technique, accompanied with detailed analysis and design equations, is proposed to maximize the achievable signal-to-noise-ratio of a 3^{rd}-order lowpass ΣΔ modulator. The proposed noise-shaping extension technique can be applied to other high-order lowpass and bandpass ΣΔ modulators. All the works have been applied to realize a low-power quadrature IF circuitry [CHE 03b] for Bluetooth receiver [BLU 99] (Chapter 7) and an ultra-low-power SC signal-conditioning systems [CHE 02a] for pacemaker applications [STO 89] (Chapter 8).

Chapter 4

CIRCUITS IMPLEMENTATION AND LAYOUT CONSIDERATIONS OF SWITCHED-OPAMP CIRCUITS

4.1 Introduction

This chapter begins with the design considerations of switchable opamps for switched-opamp circuits. The derivation of the specifications of a switchable opamp will be discussed. Due to the extra time required to turn on the switchable opamp, the operation speed of a switched-opamp circuit is slower than its switched-capacitor counterpart for a given current consumption. The fundamental turn-on time limit of a few switchable opamps reported in literatures in recent years will be discussed. To improve the turn-on time of a switchable opamp, a novel switching methodology is proposed.

Lastly, layout considerations to minimize switching noise coupling and the loading effects of parasitic capacitors to the opamp as well as layout techniques to maximize the matching of capacitors are presented.

4.2 Opamp Design Considerations for Switched-Opamp Circuits

A. Topology:
For very low voltage operation, multi-stage amplifier approach [CHE 00a][FAN 97] (by cascading gain stages to obtain high gain) is more attractive than using cascoded topology [JOH 96][GRA 93] (by cascoding transistors to obtain high output resistance for high gain), which is usually applied in conventional SC circuits operating at high voltages. The latter one provides insufficient output dynamic range due to the cascoded structure at

the output stage. Meanwhile, the former one gives a high amplification with only two transistors in the output stage, which delivers the maximal possible signal swing. The difference here becomes significant when the power supply voltage is reduced to 1-V. This is because every transistor that is cascoded in the output stage would reduce the maximum dynamic range by more than 15%.

B. Low-Frequency Gain and Phase Margin:

The low-frequency gain of the opamp must be high enough to preserve the accuracy of the circuit characteristics. A low-frequency gain of about 60 dB is usually required and sufficient for most applications. A phase margin of higher than 45° should be achieved to provide enough tolerance to process variations that may reduce the phase margin and thus affects the stability of the circuits. It would be advantageous to design the opamp with a phase margin of 45° to achieve critical damping [GRA 93] when a step signal is applied at the input of the opamp, which is connected in feedback configuration in SC circuits.

C. Unity-Gain Frequency:

The unity gain frequency is determined based on the settling time requirement and on the sensitivity of filter transfer function to the opamp gain-bandwidth. In general, the larger the unity gain frequency is, the shorter the opamp settling time and the more accurate the filter transfer function becomes. However, too high the unity gain frequency would create serious noise aliasing effect into the SC system while also dissipating extra power. In fact, to avoid excessive noise aliasing effect while preserving the filter transfer function, the unity gain frequency is generally set to be about 10 times larger than the sampling frequency of the targeted switched-capacitor circuits [GRE 86].

D. Turn-on Time of Switchable Opamp:

In accordance to the switched-opamp operation principle, the output voltage must reach its final value within a half-clock period (T/2) of time since the opamp will be off after its integration phase. This can be achieved only if the sum of the turn-on time $T_{switching\_on}$, the slew time T_{slew} and the settling time T_{settle} of the opamp is less than half a clock period as described below:

$$T_{switching\_on} + T_{slew} + T_{settle} < \frac{T}{2} = \frac{1}{2f_s}$$

As a result of the additional turn-on time requirement, switched-opamp circuits operate slower than in conventional switched-capacitor counterparts for a given current consumption. For moderate frequency operation (in less than 1-MHz operation), it is reasonable to allocate about 20% of the half-clock period for the turn-on time of the opamp. However, for high frequency operation (from a few MHz to tens of MHz), the turn-on time of a switchable opamp could be about 40% to 50% of the half-clock period. The long turn-on time is usually fundamentally limited by the turn-on mechanism of the switchable opamp. More elaboration of this fundamental limit will be provided in next section of this chapter.

a) Settling Time:
The settling time can be assumed to occupy less than 40% of the half-clock period with an accuracy of 0.1%. In general, the settling time is dependent on the –3dB bandwidth, which in turn depends on the unity-gain frequency and the closed-loop gain of the opamp, and hence it may be configuration dependent. This is because, for some opamp configurations like the folded-cascode amplifier, their unity-gain frequencies depend strongly on the load capacitance. As a result, the settling time for these amplifiers will also depend on the equivalent load capacitance when it is capacitively fed-back (usually happens in switched-capacitor and Gm-C applications). However, for a two-stage opamp, the unity-gain bandwidth and thus the settling time mainly depend on the compensation capacitor but not on the load capacitor.

b) Slew Time:
The slew time is determined by the slew rate of the opamp and the output voltage $V_{out}(t)$ change, $\Delta V_{out} = V_{out}(nT)-V_{out}(nT-T)$, that the opamp output must undergo in each integration step, as defined below:

$$T_{slew} = \frac{\Delta V_{out}}{SR}$$

It is no doubt that the largest step ΔV_{out} occurs when the signal at the highest passband frequency w_B is under processing. In the worst case, $V_{out(t)}$ will be a sampled-and–held sine wave with a frequency w_B and a hold-time of a half-clock period T/2. This is actually a result of sampling and holding a continuous time voltage $V(t)=V_{swing}\ \sin w_B t$. Hence the maximum step which $V_{out}(t)$ must take every $T=1/f_s$ seconds is given by:

$$\Delta V_{out,max} = T\left|\frac{dV(t)}{dt}\right|_{\max} = \frac{\varpi_B V_{swing}}{f_s}\ where T = \frac{1}{f_s}$$

Let x be the allowed portion of half-clock period for slew time, the slew rate requirement is given by:

$$SR \geq \frac{V_{out,\max}}{T_{slew}} \approx \frac{\varpi_B V_{swing}}{x f_s (T/2)} = \frac{2\varpi_B V_{swing}}{x}$$

Typically, x = 40% can be employed for most SC circuits employing switched-opamp technique. Note that this slew rate requirement has to be fulfilled for each of the compensation capacitors that is used in the circuit. Besides, there are of course also signals of higher frequencies than w_B present internally in the SC circuit. However, they and their harmonics fall into the stopband of the SC filter, and hence the resulting distortion will normally not affect the output signal of the whole circuit.

E. CMRR, PSRR and Noise Consideration:
Fully differential architecture is used to increase CMRR, PSRR and to minimize the noise problem. Meanwhile, the noise performance of a two-stage opamp can be improved by making a better noise performance for the first stage, given that the first stage gain is high. This is because the noise generated by later stages will be divided by the gain of the first stage when it is transferred back to calculate the equivalent input voltage noise. To achieve better CMRR, the input stage can be implemented with a differential pair, which ideally has a common-mode gain of zero. At low frequencies, the supply noise that can be coupled to the output is mainly due to variation in bias circuits and mismatches in differential structures. At high frequencies, coupling from parasitic capacitors becomes more important. To reduce the noise gain due to the parasitic capacitors, it is desirable to maximize the input and feedback capacitors and to minimize the parasitic capacitors by employing good layout techniques.

4.3 Design Review of Switchable Opamps

4.3.1 Design of Switchable Opamp by Switching Bias Current

Fig. 4.1 shows a two-stage opamp topology. The switch transistor M_{SW} can short-circuit the current mirror transistors M_{B0}, M_{B1} and M_{B2} [CRO 94]. A "High" clock signal makes the conductivity of MSW equal to zero and the current mirror acts as if M_{SW} is not present to turn on the opamp. A "Low" clock signal makes the conductivity of M_{SW} high thus drawing all the biasing current and pulling up the gate voltage of the current mirror transistors to turn off the opamp.

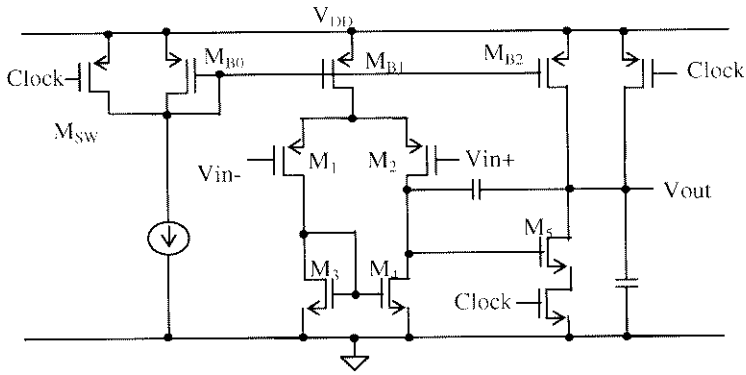


Figure 4.1 Switchable Opamp Design By Switching Bias Current

To maximize the switching speed, transistor MB0 must be made large to achieve large transconductance (gm) to charge the total gate capacitance ($C_{G,total}$) of the current mirror when turning on the opamp. The time constant associated with the current mirror is given by:

$$\tau_{turn-on} = \frac{C_{GS,total}}{gm_{MB0}}$$

It is obvious that the time constant would be minimized when the M_{B0} is as big as the total size of the other current mirror transistors M_{B1} and M_{B2}. At this condition, however, M_{B0} would dissipate as much power as the total power consumption of the opamp. Besides, since the gates of the transistors of the current mirror is to be charged by a constant current source, the switching is slow and power inefficient. In addition, the compensation capacitor is discharged during the off-phase of the opamp. In order turn on the opamp, the compensation capacitor takes long time to re-charge to its operation point due to its large time constant. Consequently, the maximal switching speed would be very limited.

4.3.2 Design of Switchable Opamp by Disconnecting from Power Rails

Another possible way to switch off an opamp is to disconnect it from the power rails [PEL 98a] as shown in Fig. 4.2. The advantage of this switching methodology is that the turn-on time is not fundamentally limited as in the case of switching the bias current as discussed in previous section. Besides, all switches could be driven by buffers, and therefore their turn-on and turn-off speed is under better control than in the bias current-switching case.

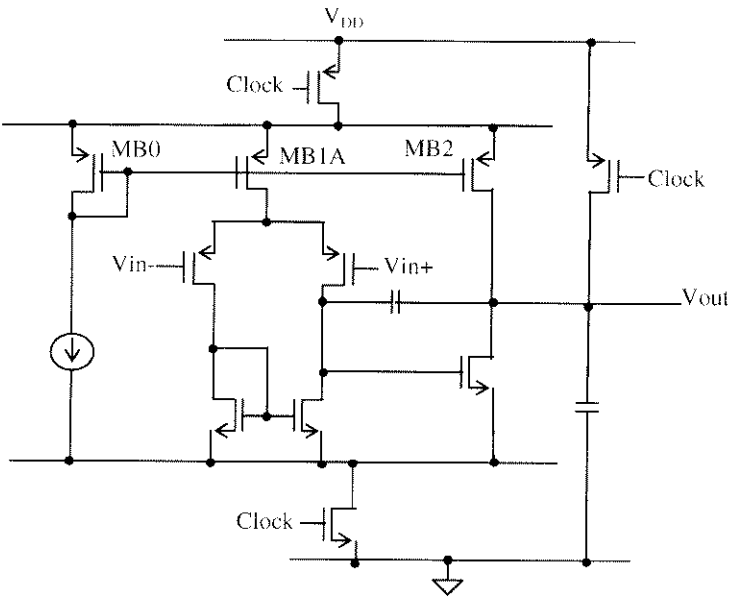


Figure 4.2 Switchable Opamp Design By Disconnecting from Power Rails

Nevertheless, this switching methodology creates a lot of switching noise to the supply and ground of the analog circuits. Moreover, the opamp takes long time to settle when it is turned on and re-connected to access the power rails.

4.3.3 Design of Switchable Opamp by Switching Output Stage

An important implication can be observed from the previous discussions that the amount of switching of the opamp circuitry should be minimized for fast switching. In fact, it is possible to switch only the output stage [BAS 97a] of a two-stage opamp to fulfil the operation principle of the switched-opamp technique as shown in Fig. 4.3. By keeping the input stage active all the time, the switching speed is now limited by the turn-on time of the current source MB3, which does not conduct current during the off-phase of the output stage. To minimize the time taken for re-charging the compensation capacitor of the two-stage opamp, switch M_{SW} is inserted to prevent the compensation capacitor from neither charging nor discharging during the off-phase of the output stage. When the output stage is turned on, the switch M_{SW} acts as the compensation resistor to remove the right-half-plane zero [GRA 93] of a two-stage opamp to achieve higher phase margin. However, additional level-shifter has to be employed to provide proper biasing of the switch MSW. As a result, the power consumption is increased.

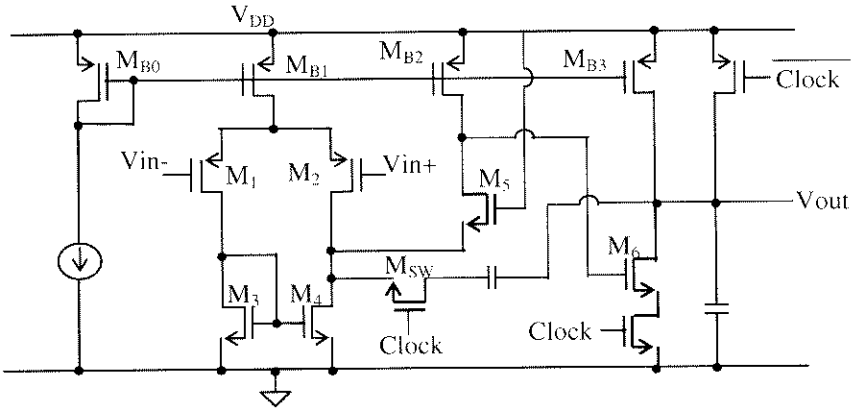


Figure 4.3 Switchable Opamp Design By Switching Output Stage

4.4 A Proposed Fast-Switching Methodology for the Design of Switchable Opamp

Figure 4.4 shows the proposed fast-switching opamp with dual time-multiplexed output stages.

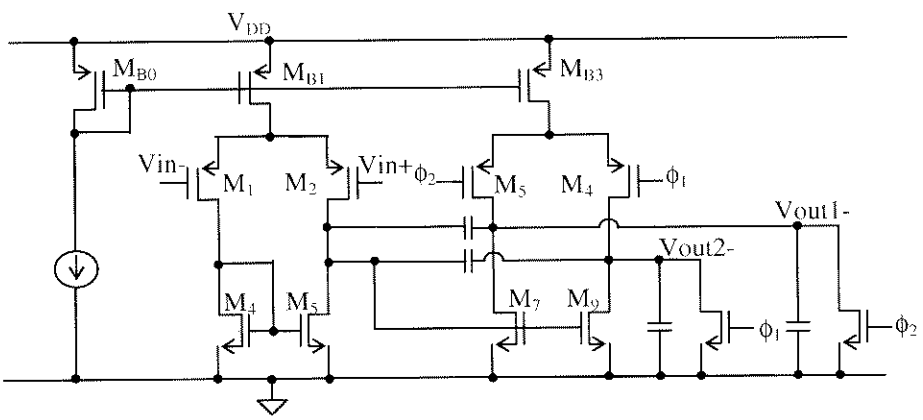


Figure 4.4 Proposed Fast-Switching Opamp with Dual Time-Multiplexed Output Stages

The two identical output stages are controlled to turn on and off alternately using the differential switches M_9 and M_{13} (M_{10} and M_{14}) with a pair of complementary clock phases (ϕ_1 and ϕ_2) [CHE 02b]. Fast turn-on time is achieved not only because the current biases M_{B2} and M_{B3} of the output stages are always kept active but also because the differential switches provide low output impedance at the turn-on instance and thus reduce

dramatically the RC time constant associated at the opamp output node. This switching methodology is most suitable to be employed for realizing the multi-phase switched-opamp technique [CHE 99], which requires two switchable opamps to work alternately such that there always exists a functional opamp. Besides, the proposed fast-switching methodology can be extended to apply on two individual switchable opamps, which work in alternate phases in the same SC system as will be described in Chapter 7. Besides, the compensation capacitors can be prevented from charging or discharging by inserting additional switches in series with them as similarly described in previous section.

4.5 Layout Considerations for Switched-Capacitor Systems

4.5.1 Layout Floorplan for Switched-Capacitor Circuits

A typical floorplan of a fully-differential switched-capacitor circuit is shown in Fig. 4.5. The analog part of the switched-capacitor circuit consists of opamps, switches and capacitors. To minimize the noise from the clocking signals to the analog part of the switched-capacitor circuit, a ground-shielded guard ring is used to provide isolation from the clock bus. For good matching of a fully-differential switched-capacitor circuit, capacitor arrays are laid out close together. Digital circuits and clock generator are laid out away from the analog part to minimize its noise coupling to the analog circuits.

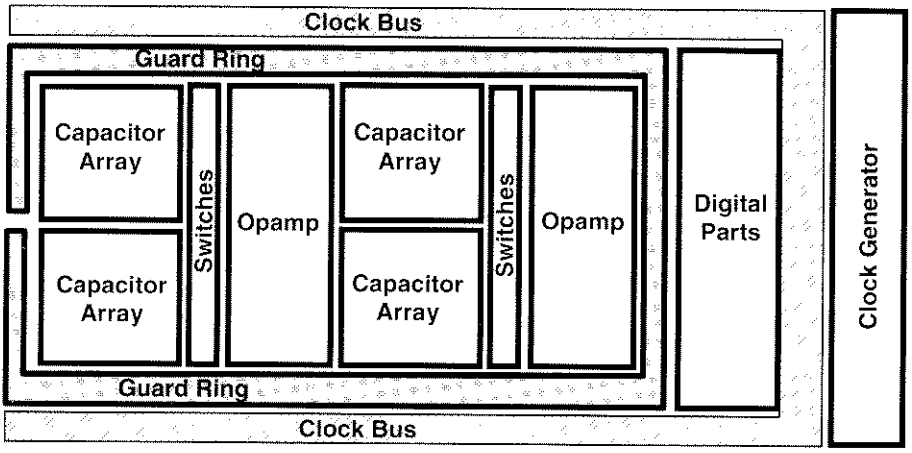


Figure 4.5 A Typical Layout Floorplan of a Fully-Differential Switched-Capacitor Circuit

4.5.2 Layout Technique for Matching Capacitors

Linear capacitors can be obtained in the TSMC 0.35-μm CMOS process with its double-poly option. The structure and the equivalent model of the linear capacitor $C_{poly\text{-}poly}$ are shown in Fig. 4.6 (a) and 4.6 (b) respectively.

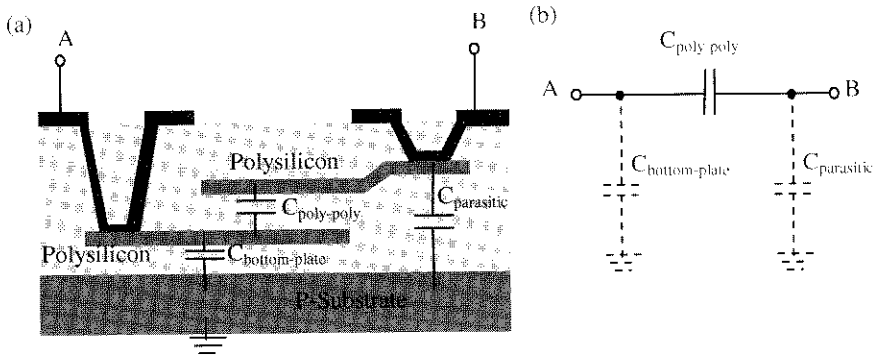


Figure 4.6 (a) Linear Capacitor Cross-Section (b) Capacitor Model with Parasitic Capacitors

The capacitor $C_{poly\text{-}poly}$ is realized across the thin oxide between the two layers of polysilicon. Bottom-plate parasitic capacitor $C_{bottom\text{-}plate}$ is formed between the bottom polysilicon layer, field oxide and the substrate, and hence its capacitance is seen at the terminal "A". The bottom-plate parasitic capacitor $C_{bottom\text{-}plate}$ has a value of about 20% of that of capacitor $C_{poly\text{-}poly}$ because of the thin field oxide between the bottom polysilicon layer and the substrate. To avoid extra capacitance loading to the opamps, the bottom plates of the capacitors should not be connected to the outputs of the opamps as will be further discussed in next section.

The best matching between capacitors can be achieved if all capacitors are designed to be an integral number of identical unit-capacitor cells. The unit-capacitor cell should be drawn in square shape to minimize the capacitance error due to the over-etching, which is proportional to the ratio of the perimeter to the area of the capacitor [LUO 99]. As the corners of the top polysilicon layer are likely to suffer from higher etching rate than the edges, the corners are made with 45° [ISM 94] to obtain a better shape control.

For good matching of two capacitors with the ratio being a non-integer, the ratios of perimeter to area of the two capacitors should be maintained the same. Consider a squared capacitor C_1 with each side being x_1 to match with a rectangular capacitor C_2 with a ratio of $C_2/C_1=K$. The two dimensions x_2 and y_2 of the rectangular capacitor C_2 are related to the capacitor ratio as:

$$K = \frac{C_2}{C_1} = \frac{A_2}{A_1} = \frac{x_2 y_2}{x_1^2}$$

where A_1 and A_2 are the areas of the capacitor C_1 and C_2. In addition, for good matching, the ratios of perimeter to area of the two capacitors should be the same:

$$K = \frac{P_2}{P_1} = \frac{A_2}{A_1} = \frac{(x_2 + y_2)}{2x_1}$$

As a result,

$$y_2 = x_1\left[K \mp \sqrt{K(K-1)}\right] = Kx_1\left[1 \mp \sqrt{1 - \frac{1}{K}}\right]$$

and

$$x_2 = \frac{Kx_1^2}{y_2} = \frac{x_1}{1 \mp \sqrt{1 - \frac{1}{K}}}$$

4.5.3 Layout Considerations for Minimizing Switching Noise Effect

Most serious noise factors of a switched-capacitor circuit are the clock signals (V_{CLOCK}) and all digital signals in a mixed-mode system like ΣΔ modulator that capacitively couple through any overlapping metal layers to the input terminal of the opamp as illustrated in Fig. 4.7 below.

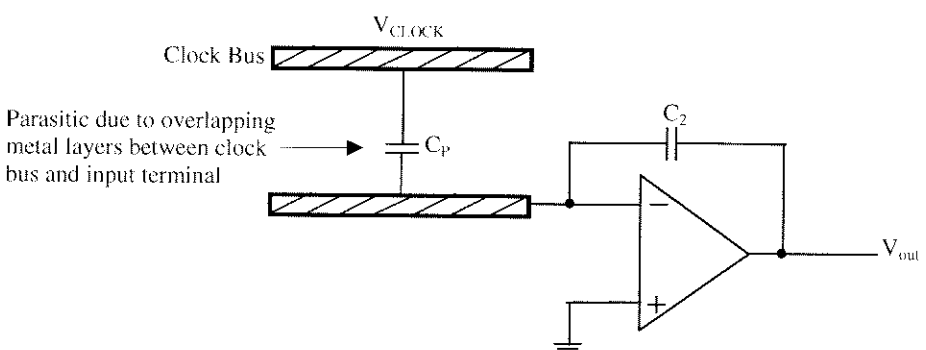


Figure 4.7 Parasitic-Insensitive Switched-Capacitor Integrators

The ideal transfer characteristic is written below:

$$\frac{V_{out}(f)}{V_{Clock}(f)} = -\frac{C_P}{C_2}$$

It can be observed that the noise signals is divided by the capacitive ratio between the parasitic capacitor C_P and the integration capacitor C_2 of the SC integrator. The seriousness of the noise coupling can be observed by considering the case where V_{Clock} = 1V, C_P = 1 fF and C_2 = 1 pF. The noise is coupled through the input terminal of the opamp to appear at V_{out} with amplitude as big as 1 mV, which would already limit the resolution of SC circuits to below 60 dB. In practice, since the parasitic capacitor could be much more than 1 fF, the noise signals that couple to the opamp output could easily go over the ten-mV range, which would kill the performance of SC circuits. As a result, this noise coupling effect must be taken into consideration when the circuit it laid out. In general, the input terminal of the opamp is too sensitive to noise that it should be kept as silent as possible and away from any large and fluctuating signal that appear in the system. Lastly, subject to the frequency of the noise signal, the effect of coupling will be less than predicted from the ideal equation 4.6 due to the finite opamp-gain-bandwidth.

4.5.4 Layout Considerations for Minimizing Parasitic Capacitive Loading to Opamp

Figure 4.8(a) illustrates the schematic of a SC integrator employing integrated capacitors with their bottom-plate parasitic capacitors connected at the output terminal of the opamp. Obviously, this adds additional capacitive load to the opamp and thus degrading the operation speed of the SC circuits. Notice that the bottom-plate parasitic capacitor C_{1P} will be added to the output of the other opamp in a SC circuits wherein a few integrators may be cascaded.

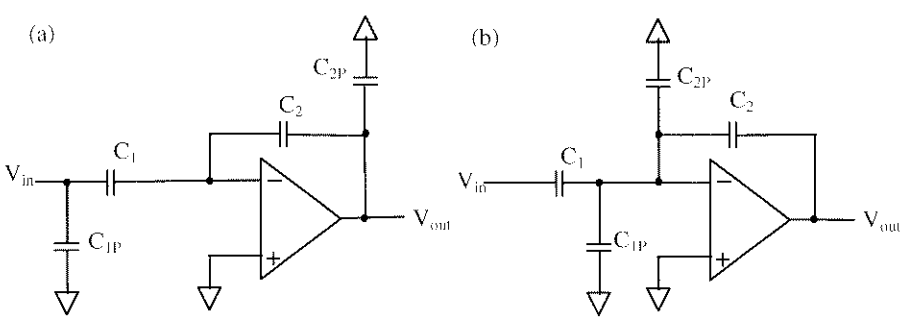


Figure 4.8 (a) Bottom-Plate Parasitic at Output of Opamp;
(b) Bottom-Plate Parasitic at Input of Opamp

On the other hand, the bottom-plate parasitic capacitors can be connected at the input terminal of the opamp as shown in Fig 4.8(b). The bottom-plate capacitors usually do not affect the transfer characteristics of the integrator if high-gain opamp is employed. By not connecting the bottom-plate capacitors at the output of the opamp, the operation speed of the SC circuits is not degraded. Nevertheless, substrate noise could be coupled to the bottom-plate of the capacitors to the opamp's input terminal, which is quite sensitive to noise as discussed before.

4.6 Conclusion

The turn-on time of a switchable opamp makes switched-opamp circuits work slower than the switched-capacitor counterpart. In general, both the settling and slew rate performance of the opamp has to be improved to compensate for the extra time spent on waking up the opamp. To improve the turn-on time of switchable opamps, different switching methodologies have been proposed in literatures. A novel switching methodology is proposed in this chapter to achieve fast-switching by maintaining the bias current active at all time so as to reduce the time to turn it on again from off-state. To improve the performance of switched-capacitor circuits, layout considerations are discussed.

Chapter 5

DESIGN OF A SWITCHED-CAPACITOR PSEUDO-2-PATH FILTER USING MULTI-PHASE SWITCHED-OPAMP TECHNIQUE

5.1 Introduction

High-Q Switched-capacitor (SC) bandpass filters can be realized with SC highpass path-filters using 2-path technique or with SC lowpass path-filters using 3-path technique [VON 83][ANA 95]. Though the 2-path filter offers better filter performances while employing less path cells, the required SC highpass ladder filters have generally stray-sensitive structures unless those stray-sensitive switching capacitor branches are replaced by opamps [GER 86], which certainly increases the power consumption and therefore is not desired. Meanwhile, SC lowpass ladder filters usually have stray-insensitive structures [GER 86][ANA 95], and thus a trade-off between power consumption and filter performances seems unavoidable when choosing between 2-path filter and 3-path filter topologies. However, in z-domain, a lowpass response can be transformed to a highpass response by replacing all "z" terms in the transfer function with "-z", which is known as the "z to –z transformation". By employing z to –z transformation on a switched-capacitor lowpass filter, a highpass filter can be obtained while inherently enjoying the advantages of the lowpass ladder filter structure without asking for extra.

In practice, an LDI-transformed lowpass ladder filter is firstly derived and converted to a highpass ladder filter using z to –z transformation method [PAT 81][RAN 85][BET 90][SHA 91]. A z to z^N transformation, which further converts the highpass filter into a bandpass filter, can then be realized through employing a RAM-type pseudo-N-path integrator cell [PAL 89a]. However, at a low supply voltage, the design of RAM-type path cell is infeasible to be constructed using the original switched-opamp technique, which does not provide multi-phase operation since its operation principle

requires to shut down the opamps after their integration phases. To solve the problem, the multi-phase switched-opamp technique is proposed and demonstrated a low-voltage switched-opamp RAM-type path cell to implement a 1-V SC pseudo-2-path filter in this chapter.

5.2 N-Path and Pseudo-N-Path Filters

5.2.1 N-Path Filter

To achieve very high Q-values (relative bandwidth of 1% or less) bandpass filter response, design technique based on the N-path filter concept may be used [VON 83][RAN 85][BET 90][SHA 91]. The N-path technique makes use of the alias and image frequency-translated responses of SC filters in order to achieve highly selective bandpass responses using low sensitivity SC filters with low capacitance spread. To explain the principles of N-path filters we consider the amplitude response A_{SCLP} of a switched-capacitor lowpass filter (SC-LPF) as shown in Fig. 5.1. This SC-LPF is a sample-data network and is sampled with the clock frequency f_c. The resulting periodical frequency response A_{SCLP} has a bandpass characteristic related to the low-pass filter at multiples of the clock frequency f_c. This characteristic suggests the use of the low-pass filter as a bandpass filter. As stated by the Nyquist theorem, sampled data filters can only correctly process any input signal up to the half of the sampling frequency f_c. The frequency range is referred to as the Nyquist range (NY).

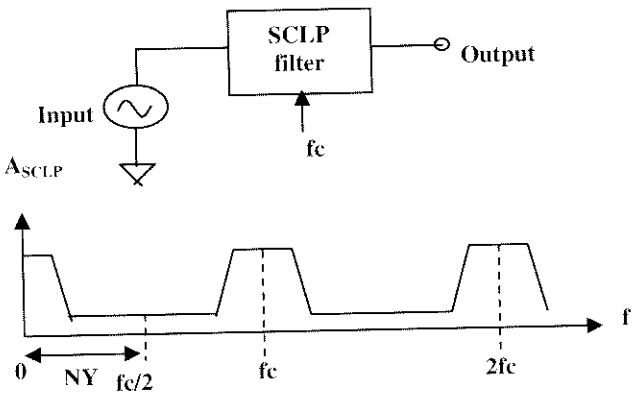


Figure 5.1 Amplitude Response (ASCLP) of an SC Lowpass Filter

In fact, we can increase the Nyquist range of the SC lowpass filter by increasing the number (N) of samples per period. This can be achieved by using additional paths (not by over-sampling alone, as this will only enlarge

the whole frequency response). Such an expanded filter is called an N-path filter. Figure 5.2 shows an N-path (N=3) filter.

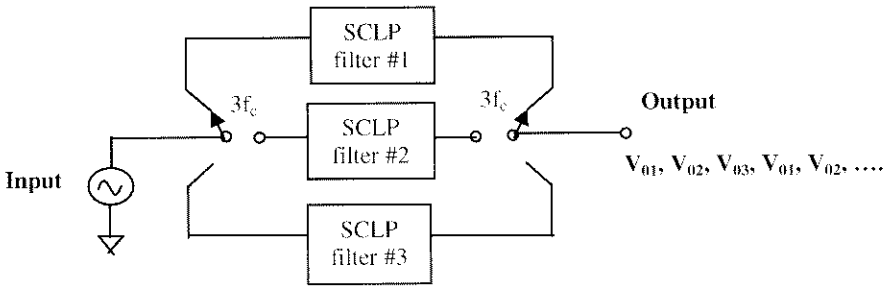


Figure 5.2 N-path Filter Structure Consisting of N Parallel, Identical, and Cyclically Sampled Lowpass Filter Cells with the Corresponding Clock Scheme (N=3 is Shown)

The N-path (N=3) filters consist of 3 parallel identical filter cells, which are cyclically sampled with the frequency f_c. As such, the 3 path-filters take turn to give out its output signal V_{01}, V_{02}, V_{03}, V_{01}, V_{02}, and so and so for. As such, the transfer characteristic as seen from the output node is the same for every switch position, and so the overall frequency response of the N-path filter is equal to the response of an individual path, which is a lowpass response in this case. However, the output signal is now composed of N samples per period, so that the Nyquist range for the N-path filter is expanded by N times. The situation can be presented graphically as shown in Fig. 5.3.

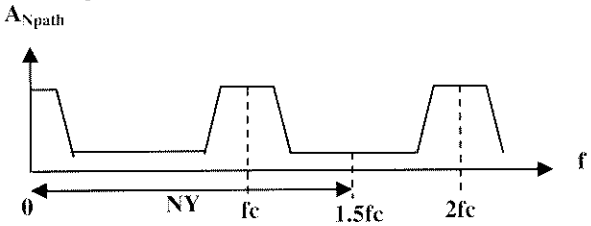


Figure 5.3 Amplitude Response (Anpath) of an N-Path Filter with N=3

Now the Nyquist range (NY) has been extended by 3 times (since N=3 is used) to cover the bandpass response that centered at frequency f_c. With the use of appropriate lowpass pre-filter and bandpass post-filter, such an expanded SC low-pass filter can be used as a bandpass filter with the center frequency at f_c. Unlike the case of using over-sampling to expand Nyquist range, the amplitude response of the N-path filter is the same as that of the lowpass filter though N times higher sampling rate is used to operate the filter. Therefore, the overall transfer function of N-path filter has the same filter coefficients and, accordingly, identical sensitivities as an individual filter path cell. More importantly, since the path cell is a lowpass filter, the sensitivities to element value variations and the resulting capacitance spread

are much less than that of a conventional SC bandpass filter that implements the same transfer function as that of the N-path filter. This is one of the most important advantages of using SC N-path filters over the conventional SC bandpass filters. The low sensitivity to element value tolerances of this approach allows the design of bandpass filters with quality factor (Q - value) up to a few hundreds with acceptable yield and capacitance spread. Besides, since the center frequency of the passband is equal to a multiple of the clock frequency, a very stable and exact center frequency can be obtained. Meanwhile, by controlling the clock frequency, the center frequency of the filter can be adjusted, thus the N-path filter is tunable [PAT 81]. However, the N-path filter also brings out several important shortcomings:

1. The MOS switches used in SC filters introduce clock feedthrough signal at the output. This clock feedthrough signal produces not only an undesirable offset voltage, but also additional spectral components at integer multiples of the clock frequency f_c. These spectral components reduce the maximum dynamic range in the filter passband at f_c, since the clock feedthrough noise falls into the passband of the filter.

2. Another disadvantage of N-path filters is that N times more components are needed and hence approximately N times more power consumption.

3. Besides, any asymmetry among the path filters introduces spurious output signals and mirror frequency noise.

The clock feedthrough noise can be eliminated for N-path filter that uses highpass filter as filter path cell instead of lowpass one [RAN 85][BET 90][FRA 91]. To explain this, we consider the amplitude response of a SC highpass filter (SC-HPF) as shown in Fig. 5.4.

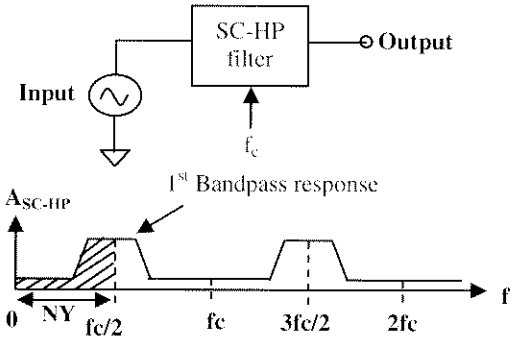


Figure 5.4 Amplitude Response (ASCHP) of a SC Highpass Filter

For a highpass resposnse, the Nyquist range only covers up to half of the sampling frequency, and hence the bandpass response centered at $f_c/2$ cannot be used. In order to utilize the first bandpass response, we can build a N-path (N=2) filter with two highpass filters as path cells, which is shown in Fig. 5.5 below.

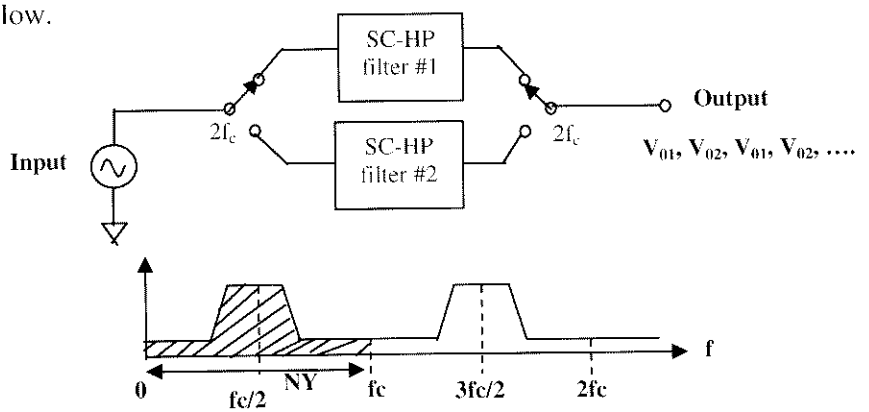


Figure 5.5 N-Path Filter Structure Consisting of N Parallel, Identical, and Cyclically Sampled Highpass Filter Cells with the Corresponding Clock Scheme (N=2 is Shown)

By so doing, the Nyquist range is extended to cover signal frequencies up to f_c, and hence the whole bandpass response can be used. Here, the passbands lie at frequencies $f_o=if_c/2$ (i =1,3,5...) while the clock frequency components are located at integer multiples of f_c. As a result, the clock feedthrough noise do not appear in the passbands and therefore can be filtered out by applying approriate post-filter, which is a lowpass filter if the first passband is desired to use.

5.2.2 Pseudo-N-Path Filter

Though N-path filter can achieve a bandpass response with Q-values as high as a few hundreds, they are power hungry as N paths are needed and hence N times more components are required. The main idea of pseudo-N-path filter [GER 86][PAL 89a][PAL 89b][SHA 92][SHA 94] is that since only one of the path filters is active at any given time, it is therefore worthy to time share all memoryless elements of the path filters, that is, opamps and the switched capacitors which are fully discharged in each cycle. Such timesharing is advantageous not only because it saves components, but it also eliminates some potential sources of path asymmetry that causes spurious output signals and mirror-frequency noise, since now the same opamps and switched capacitors can be used in all paths. A table of comparison between the properties of N-path filter and pseudo-N-path filter (using lowpass path cell or highpass path cell) can be readily obtained. This is shown in Table 5.1 below.

Table 5.1 Comparisons on N-Path and Pseudo-N-Path Filter Using Lowpass Path Cells and Highpass Path Cells

Parameters	N-Path Filter		Pseudo-N-Path Filter	
	Lowpass path cell	**Highpass path cell**	**Lowpass path cell**	**Highpass path cell**
Sampling frequency (f_s)	$N_{LP}f_c$	$2N_{HP}f_c$	$N_{LP}f_c$	$2N_{HP}f_c$
Center frequency (f_c) of resulting bandpass response	f_s/N_{LP}	$f_s/2N_{HP}$	f_s/N_{LP}	$f_s/2N_{HP}$
Bandwidth of resulting bandpass response	$2f_p$	$2(f_s-f_h)$	$2f_p$	$2(f_s-f_h)$
Minimum number of paths	3	2	3	2
Clock feedthrough	Yes	No	No**	No
Pre-filtering	Bandpass	Lowpass	Bandpass	Lowpass
Post-filtering	Bandpass	Lowpass	Bandpass	Lowpass
Number of Opamps needed (in multiple of that required in a path filter)	N times	N times	Same	Same

** Where f_p and f_h stand for passband edges for lowpass and highpass filters respectively.*
*** Pseudo-N-path filter using lowpass path cells can be made free from clock feedthrough noise by using circulating delay type cells [PAL 89b]*

5.3 Z to -Z^{-N} Transformation Using RAM-Type SC Pseudo-N-Path Integrator

One elegant way of constructing a SC pseudo-N-path filter is to replace those SC integrators that employed in a lowpass filter topology with a RAM-type SC pseudo-N-path integrator [PAL 89a], which achieves z to $-z^N$ transformation on a conventional SC integrator. An example of a RAM-type SC pseudo-2-path integrator is shown in Fig. 5.6.

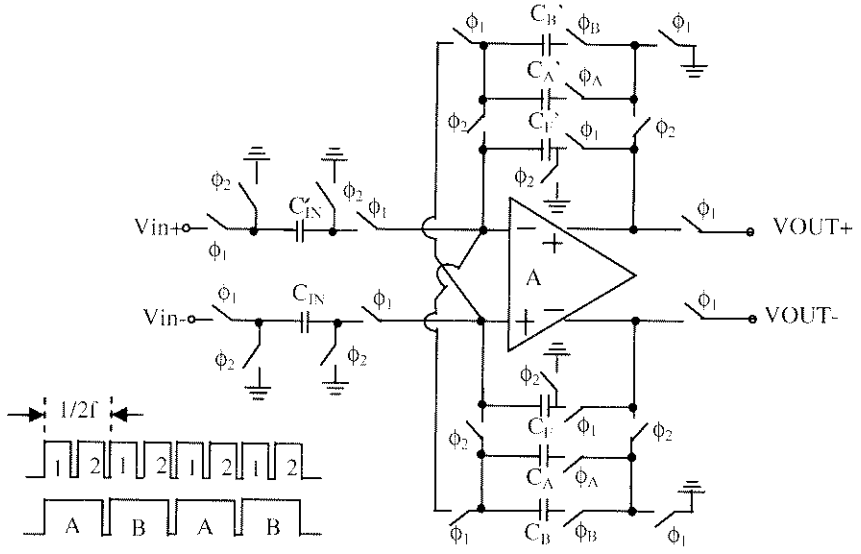


Figure 5.6 Differential Pseudo-2-Path Transformed SC Integrator

The capacitors C_F and C_F' are the differential integrating capacitors of a conventional SC integrator. The capacitors C_A and C_A', and C_B and C_B' work as the only storage elements in this circuit. The operation is as follows. During ϕ_A, the RAM-type path cell is integrating the new signal and the stored signal in capacitors C_A and C_A' at ϕ_1, the resultant signal is passed back and stored in storage capacitors C_A and C_A' at ϕ_2. The circuit works similarly at ϕ_B but with C_B and C_B' as the storing elements. Now, assume all capacitors in the differential paths are perfectly matched, at phases ϕ_A and ϕ_1, capacitor C_F (C_F') receives the charge from the input capacitor C_{IN} (C_{IN}') and from the storage capacitor C_A' (C_A) from the opposite path. This operation gives the sign inversion required by the z to -z transformation to the integrator. During the time when both ϕ_A and ϕ_2 are on, the updated charge in C_F (C_F') is transferred back to C_A (C_A') in the storage array. This charge is then held on C_A (C_A') for *two sampling periods*. Equation 5.1 presents the operation of C_A mathematically.

$$\left.\begin{aligned} Vout^{+}(nT) &= \left(\frac{C_A}{C_F'}\frac{C_F}{C_A}\right)Vout^{-}(nT-2T) - \frac{C_{IN}'}{C_F'}Vin(nT)^{+} \\ Vout^{-}(nT) &= \left(\frac{C_A}{C_F}\frac{C_F'}{C_A}\right)Vout^{+}(nT-2T) - \frac{C_{IN}}{C_F}Vin(nT)^{-} \end{aligned}\right\} \qquad \text{(Eq. 5.1)}$$

Similarly, the same operation is repeated during phase ϕ_B while the charge is stored on C_B (C_B'). By doing so, z to $-z^2$ transformation is resulted. Equation 5.2 mathematically describes the operation on capacitor C_B.

$$\left.\begin{aligned} Vout^{+}(nT+T) &= \left(\frac{C_B}{C_F'}\frac{C_F}{C_B}\right)Vout^{-}((nT+T)-3T) - \frac{C_{IN}'}{C_F'}Vin(nT+T)^{+} \\ Vout^{-}(nT+T) &= \left(\frac{C_B}{C_F}\frac{C_F'}{C_B}\right)Vout^{+}((nT+T)-3T) - \frac{C_{IN}}{C_F}Vin(nT+T)^{-} \end{aligned}\right\} \qquad \text{(Eq. 5.2)}$$

Equation 5.3 describes the transfer function of the RAM-type SC pseudo-2-path integrator, which is derived by performing z-transformation on either Equation 5.1 or 5.2, since both equations give the same result towards z-transformation.

$$\frac{Vout^{+} - Vout^{-}}{Vin^{+} - Vin^{-}} = -\frac{C_{IN}}{C_F\left(1+z^{-2}\right)} \qquad \text{(Eq. 5.3)}$$

It can be observed that the RAM-type SC pseudo-2-path integrator has successfully transformed the equation of a conventional SC integrator with a z to $-z^2$ transformation. Such an arrangement would basically guarantee the memory elements, such as the integrating capacitors in SC circuits, are properly handled to achieve z to $-z^N$ transformation. For some SC systems that involve memory elements other than the integrating capacitors, such as an elliptic SC ladder filter architecture, minor modifications are needed. This will be explained further in section 5.4. A useful design consideration of the storage capacitors C_A and C_B of the RAM-type SC pseudo-2-path integrator can be observed through Equations 5.1 and 5.2, which show that the transfer function is independent to the values of capacitor C_A and C_B. It is however optimized to use same size capacitors for C_F, C_F', C_A, C_A', C_B and C_B'. It is because if the storage capacitors (C_A, C_A', C_B and C_B') are smaller than the integrating capacitors (C_F and C_F'), the signal will be amplified by the ratio (C_A/C_F or C_B/C_F) when it is stored. Therefore requiring more signal dynamic range from the opamp to prevent it from being distorted. Meanwhile, using storage capacitors that are larger than the integrating capacitor will slow down the speed of operation, and this is also not desired in the chip-area point of view.

5.4 Design of a 1-V Switched-Opamp SC Pseudo-2-Path Filter

Figure 5.7 shows a switched-opamp RAM-type pseudo-2-path integrator [CHE 00b] using the proposed multi-phase switched-opamp technique described in section 2.5.

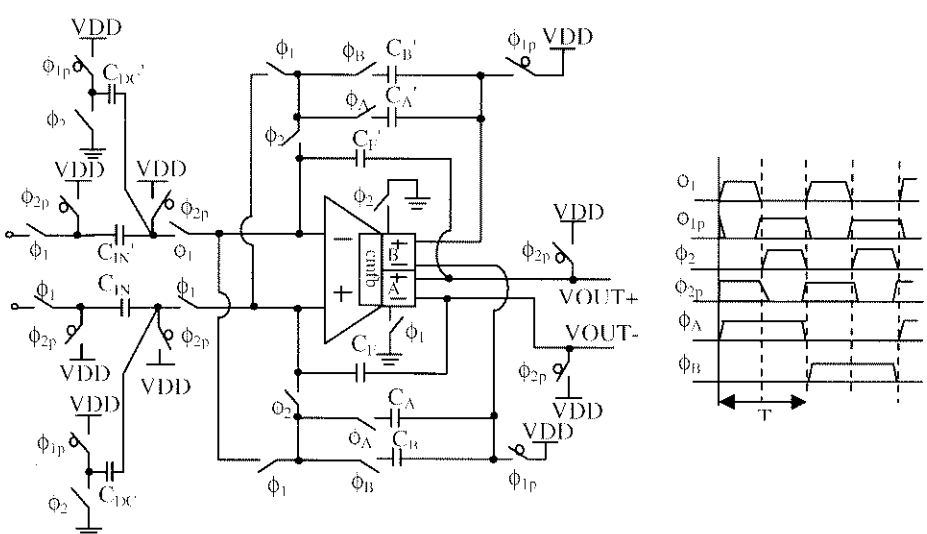


Figure 5.7 Differential RAM-Type Pseudo-2-Path Integrator Using the Proposed Multi-Phase Switched-Opamp Technique [CHE 00b]

C_F and C_F' are the integrating capacitors while C_A (C_A') and C_B (C_B') are for the storage array. When ϕ_A and ϕ_1 are on, output pair A is turned on to connect C_F and C_F' in feedback configuration while output pair B is off with its outputs shorted to V_{DD}. C_F (C_F') receives the charge from C_{IN} (C_{IN}') and from C_A' (C_A) from the opposite path. This operation gives the sign inversion required by the $z \rightarrow -z$ transformation [PAL 89b][SHA 92]. When ϕ_A and ϕ_2 are on, output pair B is turned on to connect the storing capacitors C_A and C_A' in feedback configuration while output pair A is turned off with its outputs shorted to V_{DD}. In this way, the updated charge in C_F (C_F') is transferred back to C_A (C_A'). This charge is then held in C_A (C_A') for two sampling periods. The same operation is repeated during ϕ_B with the charge stored in C_B (C_B') instead of C_A (C_A'). By doing so, $z \rightarrow -z^2$ transformation is successfully realized with the fully-differential two-switchable-output-pair opamp.

Figure 5.8 shows the schematic of the switched-opamp SC pseudo-2-path filter [SHA 92], which is synthesized by replacing the integrators in a conventional elliptic 3rd-order SC lowpass ladder filter [GER 86] with the switched-opamp RAM-type pseudo-2-path integrator. A fully-differential structure not only helps reject common-mode noise and reduce clock-feedthrough noise but also provides a free sign inversion of the output voltages, which is required in the overall $z \rightarrow -z^2$ transformation. Since only one pair of output stages is active at a time, the resulting 1-V SC pseudo-2-path filter uses the same number of opamps as its classical counterpart.

It is important to notice that some minor modifications are needed for the coupling capacitors C_{21} (C_{21}') and C_{22} (C_{22}'), since they are also memory elements in the system that realize z-transfer function of the type $(z^{-1}-1)$. Therefore, when the z to $-z^2$ transformation is used, their transfer functions have to change to be $(-z^{-2}-1)$. This can be achieved by connecting the bottom plates of these coupling capacitors, which were originally connected directly to the amplifier output nodes [GER 86] in the lowpass ladder filter, to the switched nodes [PAL 89b]. In this case, the charge on these coupling capacitors is temporarily stored on the integrating capacitors C_A (C_A') and C_C (C_C'), and will be given back after each sampling periods.

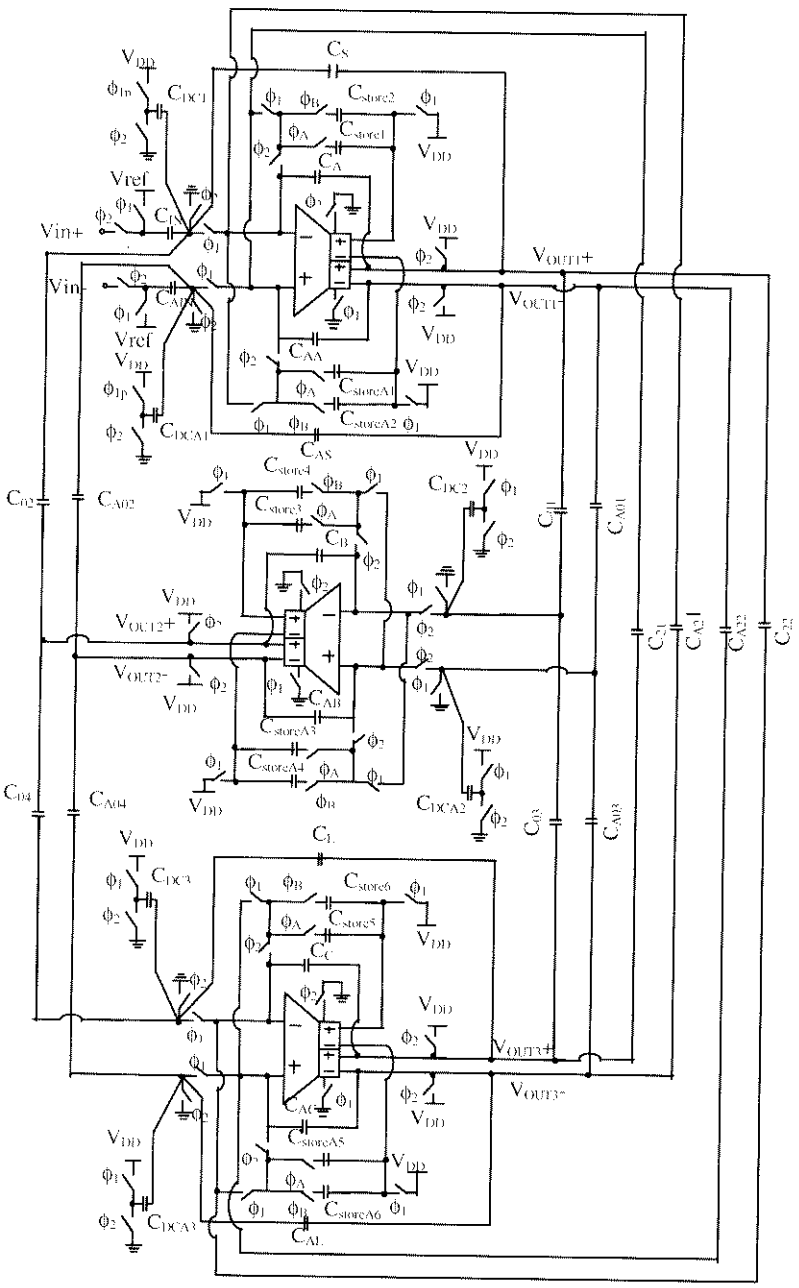


Figure 5.8 SC Pesudo-2-Path Filter Using the Proposed Multi-Phase Switched-Opamp Technique

5.5 Circuits Implementation

Figure 5.9 shows the schematic of the proposed 1-V fully-differential two-output-pair switchable opamp. The opamp is implemented with HP 0.5-μm CMOS N-well process with NMOS and PMOS threshold voltages of 0.7 V and 0.85 V respectively. A PMOS differential pair is used as the input stage for smaller Flicker noise [HUN 90][VAN 94].

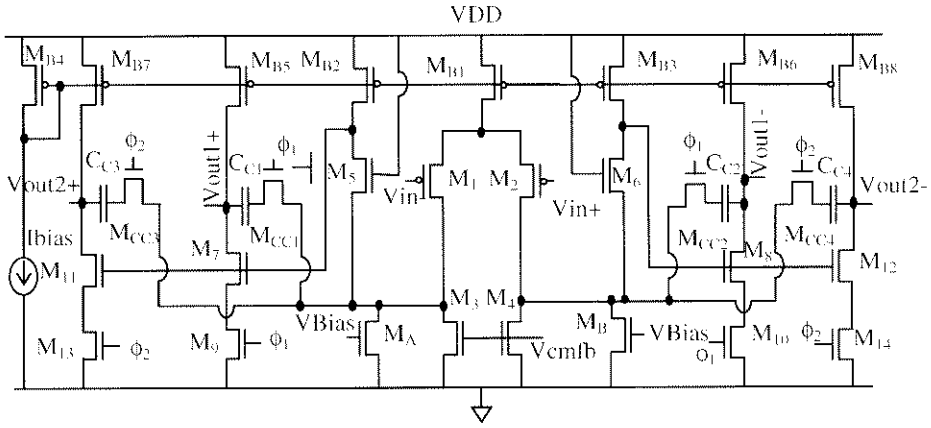


Figure 5.9 Schematic of the Proposed Fully-Differential Two-Switchable-Output-Pair Opamp

To cope with the already tight voltage budget, the body effect that tends to increase the threshold voltage of the PMOS input transistors has to be eliminated by connecting the PMOS bodies to their sources. This is possible in N-well process when the PMOS input transistors are laid-out with a separate N-well from other PMOS transistors. In order to obtain a low frequency gain of better than 75 dB to maintain the filter transfer function accuracy, this is necessary to ensure that both input (M_1 and M_2) and load (M_3 and M_4) transistors operate in saturation region. Therefore, the gates of output stage transistors (M_7, M_8, M_{11} and M_{12}) are not connected directly to the output nodes of the input stage as in the case of conventional two-stage opamp configuration. Instead, level shifters formed by M_5, M_{B2} and M_6, M_{B3} respectively are inserted in between such that M_3 and M_4 are biased with one V_{DSsat} higher than ground while ensuring M1 and M_2 operate in saturation region [BAS 97a][CHE 00b]. Capacitors C_{C1}, C_{C2}, C_{C3} and C_{C4} are compensation capacitors for the two pairs of output stages. The output stages are turned on and off by the transistors M_9, M_{10}, M_{13} and M_{14}, which are controlled by the two non-overlapping clock phases ϕ_1 and ϕ_2. When the output stages are cut-off, compensation resistors M_{CC1} and M_{CC2} (or M_{CC3} and M_{CC4}) are turned off to prevent the compensation capacitors from discharging or charging up for faster switching operation. Since the switches that connect at the outputs of opamps in the proposed 1-V SC pesudo-2-path filter are tied

to V_{DD} when the output stages are in off phase, thus preventing static current from flowing through those switches and the output stages.

Figure 5.10 shows a dynamic common-mode feedback circuitry, which can adjust the output common-mode voltages to 0.5 V (middle of rails) by negatively feeding back signal to the gates of transistors M_3 and M_4. Transistors M_A and M_B are used to adjust the common-mode feedback loop-gain by drawing currents from M_3 and M_4 respectively. As such the transconductance of M_3 and M_4 can be adjusted. Table 5.2 summarizes the transistor sizes of the proposed switchable opamp.

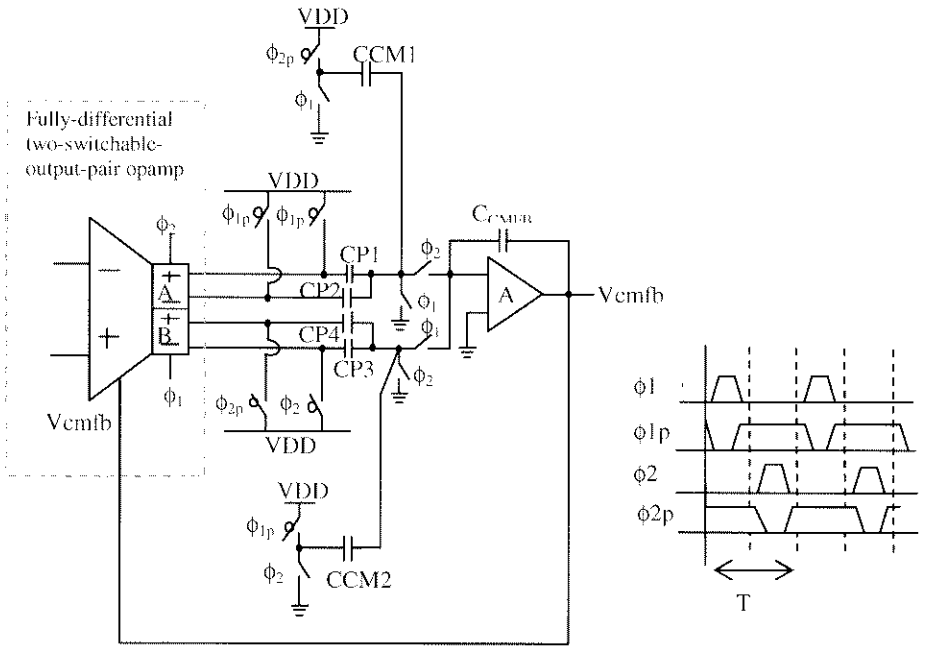


Figure 5.10 Dynamic Common-Mode Feedback Circuit for the Fully-Differential Two-Switchable-Output-Pair Opamp

Table 5.2 Summary of Transistors Sizes of Switchable Opamp

Transistors	Unit size	Quantity
M_1, M_2	12μm/2.1μm	12
M_3, M_4	3μm/3μm	12
M_A, M_B	3μm/3μm	20
M_5, M_6, M_7, M_8, M_{11}, M_{12}	3.3μm/2.1μm	20
M_{B4}	10.2μm/2.1μm	4
M_{B1}	10.2μm/2.1μm	24
M_{B2}, M_{B3}, M_{B5}, M_{B6}, M_{B7}, M_{B8}	10.2μm/2.1μm	20
M_9, M_{10}, M_{13}, M_{14}	3.3μm/2.1μm	8
M_{CC1}, M_{CC2}, M_{CC3}, M_{CC4}	5.1μm/0.6μm	10

It is worth to mention that, with a single 1-V supply, the input common-mode voltage of the switchable opamp has to be set at ground, which results in zero input common-mode range. But this is not critical to the operation of SC circuits, since the inputs of opamps are operating near the virtual ground in steady state, therefore no input common-mode range is required. Table 5.3 summarizes the measured performance of the switchable opamp.

Table 5.3 Measured Performance of the Switchable Opamp

Technology	0.5-μm CMOS
Supply Voltage	1 V
Low Frequency Gain	69 dB
Unity Gain Bandwidth	7 MHz
Phase Margin	45°
Power Consumption	80 μW
Chip Area	100 μm x 50 μm

5.6 Experimental Results

Figure 5.11 shows the chip photograph of the filter, which occupies an area of 0.8 mm^2 with unit capacitors of 0.1pF and a capacitance spread of 50. The filter is implemented with a single-poly triple-metal 0.5-μm CMOS process.

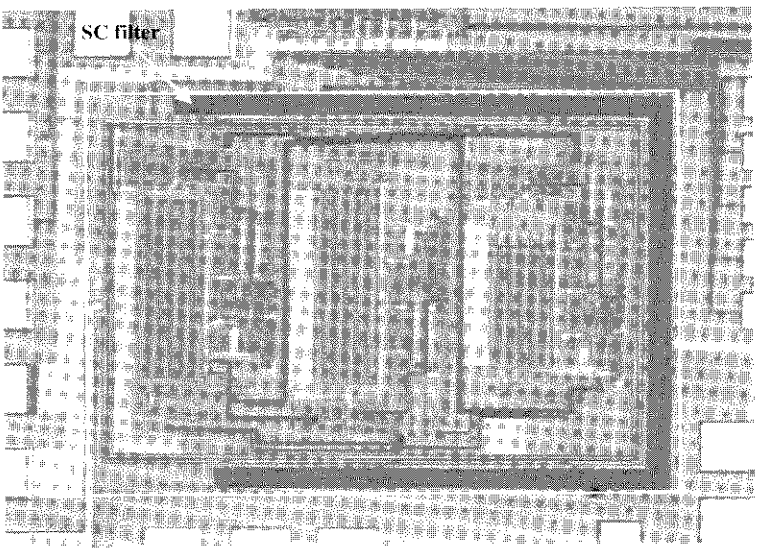


Fig. 5.11 Die photo of the filter

The capacitors are formed with polysilicon and highly doped N-well (cap-well option) regions to achieve both good linearity and small chip-area (2 $fF/\mu m^2$). The main drawback of using such a linear capacitor is that a large bottom-plate parasitic capacitor of about 1/4 size of the linear capacitor is created between the highly doped N-well and the P-type substrate. To minimize the loading effects of those large bottom-plate parasitic capacitors, special care should be taken in the layout to avoid the bottom-plate of the linear capacitors to connect to the opamp outputs. Table 5.4 summarizes the capacitor values used.

Table 5.4 Summary of Capacitor Values

C_A, C_{AA}, $C_{storeA1}$, $C_{storeA1}$, C_{store2}, $C_{storeA2}$	4.5pF	C_{02}, C_{A02}, C_{03}, C_{A03}	0.1pF
C_B, C_{AB}, C_{store3}, $C_{storeA3}$, C_{store4}, $C_{storeA4}$	5pF	C_{01}, C_{A01}	0.15pF
C_C, C_{AC}, C_{store5}, $C_{storeA5}$, C_{store6}, $C_{storeA6}$	3.5pF	C_{21}, C_{A21}	0.13pF
C_{IN}, C_{AIN}	0.59pF	C_{22}, C_{A22}	0.21pF
C_S, C_{AS}	0.14pF	C_L, C_{AL}	0.1pF
$C_{DC1} = (C_S+C_{02})/2$, $C_{DCA1} = (C_{AS}+C_{A02})/2$		0.17pF	
$C_{DC2} = (C_{01}+C_{03})/2$, $C_{DCA2} = (C_{A01}+C_{A03})/2$		0.13pF	
$C_{DC3} = (C_L+C_{04})/2$, $C_{DCA} = (C_{AL}+C_{A04})/2$		0.1pF	

The measured transient responses for a single-ended output and the differential output of the filter with a 75-kHz 0.3-V_{pp} in-band input are shown, respectively, in Fig. 5.12(a) and 5.12(b). The corresponding frequency spectrum for the differential output signal is shown in Fig. 5.12(c).

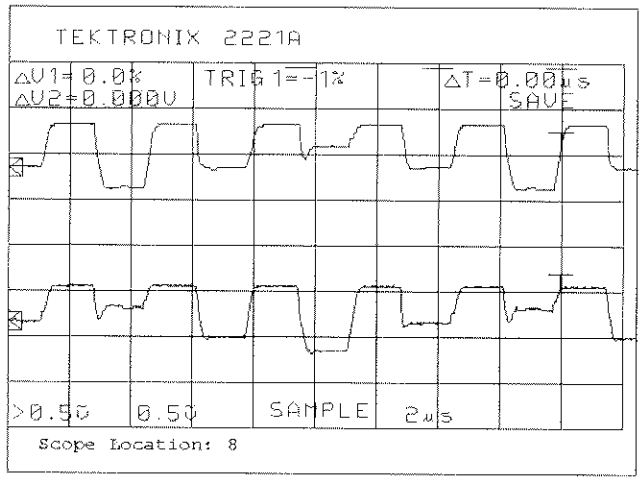


Figure 5.12 (a) Single-Ended Output Transient Response with a 75-kHz 0.3-V_{pp} Input Signal

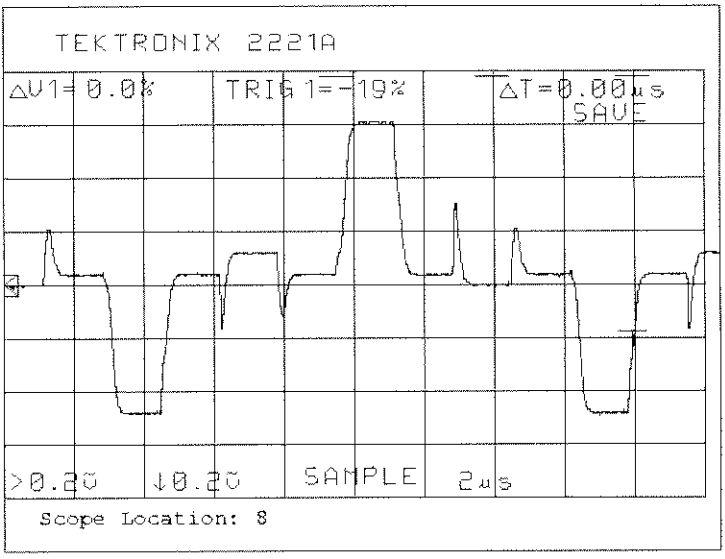


Figure 5.12 (b) Differential Output Transient Response with a 75-kHz 0.3-V_{pp} Input Signal

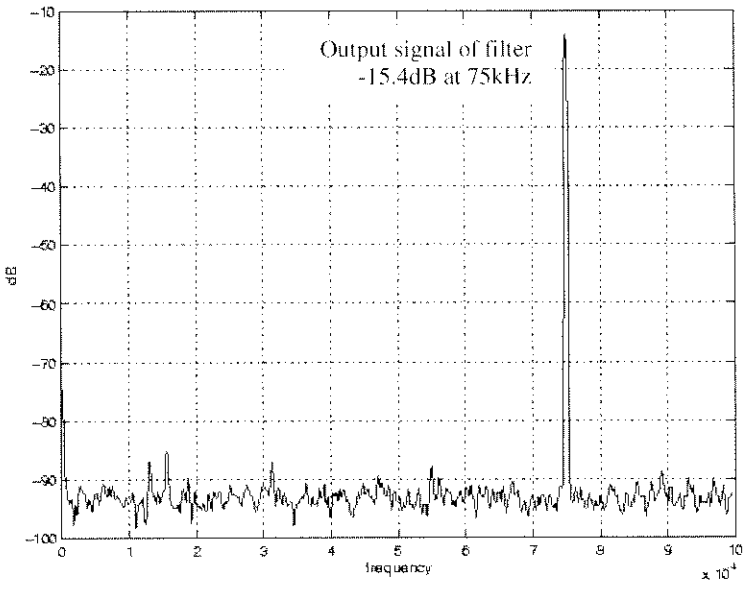


Fig. 5.12 (c) Frequency Spectrum with a 75-kHz 0.3-V_{pp} Input Signal

It can be observed that the filter settles properly even for a differential output signal amplitude as large as 1.2 V_{pp}. From the above waveforms, it is evident that the proposed switched-opamp mechanism is also based on the fact that during one clock phase the output node is tied to the power supply and the output signal is not available, which is the same as in the case of the previous switched-opamp technique. This causes a return-to-zero effect, which reduces the passband gain of the filter by 6 dB [BAS 97a] if the signal is processed continuously. Hence, it must be taken into account when the filter passband gain is designed. In order to fully utilize the output swing of the proposed filter prototype, the filter is designed to achieve about 10 dB passband gain for sampled-and-held output signal waveforms. In this case, the peak-to-peak filter output signal is about 4 times of that of the input signal in the passband. This is because the input signal swing of the filter is limited to be less than 0.3 V_{pp} due to the turn-on requirements of the input switches.

Theoretically, the maximum input signal amplitude is limited to be less than 0.4 V_{pp} if NMOS ($V_T \sim 0.7$ V) switch is used and the clock voltage is same as the supply voltage (1 V). Certainly, the on-resistance of the input switch is signal dependent. The required on-resistance of the input switch is determined by the RC time constant requirement during the sampling phase for realizing a sufficient input signal bandwidth and proper settling at the end of each sampling instance. The drawback of this design is that the input switch is made large in order to enlarge the input signal swing while achieving a low on-resistance but increasing the charge injection and clock feedthrough noise. However, thermal noise contribution by the first sampling switch will be decreased since most of the time the on-resistance of the input switch is lower than required.

Figure 5.13 shows the measured frequency response of the filter. The filter achieves a 6^{th}-order bandpass response with a bandwidth of 1.7 kHz and a passband gain of 1 dB. A minimum stopband loss relative to passband of –38 dB is measured at frequencies of 72.5 kHz and 77.5 kHz. As a property of a pseudo-2-path filter, the center frequency of the interested passband is accurately located at 75 kHz, which is exactly 1/4 of the sampling frequency (300 kHz), as desired. The filter actually could still settle properly for sampling frequencies up to 800 kHz. Besides, power consumption could still be increased to achieve faster operation if necessary.

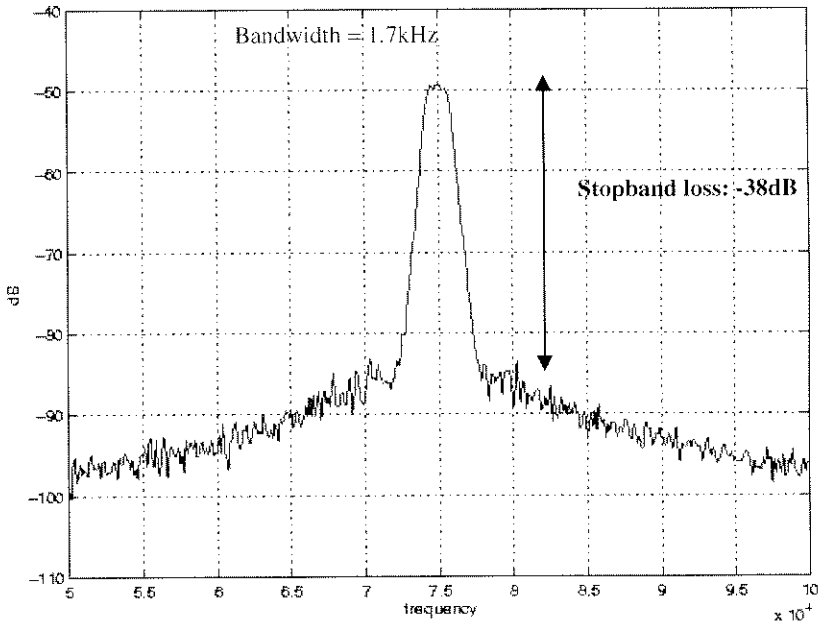


Figure 5.13 Frequency Response of the SC Pseudo-2-Path Filter

The third-harmonic distortion is measured with an in-band continuous input signal at frequency at f_{in} = 75.3 kHz. The third-harmonic component of the input signal is located at $3*f_{in}$ = 225.9 kHz and is folded at $f_s - 3*f_{in}$ = 74.7 kHz, which is in the passband of the filter. Figures 5.14(a) and 5.14(b) show the measurement results for 1% and 3% total harmonic distortion (THD) respectively. The 1% THD corresponds to a 0.42-V_{pp} input signal and the 3% THD to a 0.45-V_{pp} input signal. The measured total output noise of the filter is about 1 mV_{rms}. The dynamic range for 3% THD is about 54 dB. Table 5.5 summarizes the filter performance.

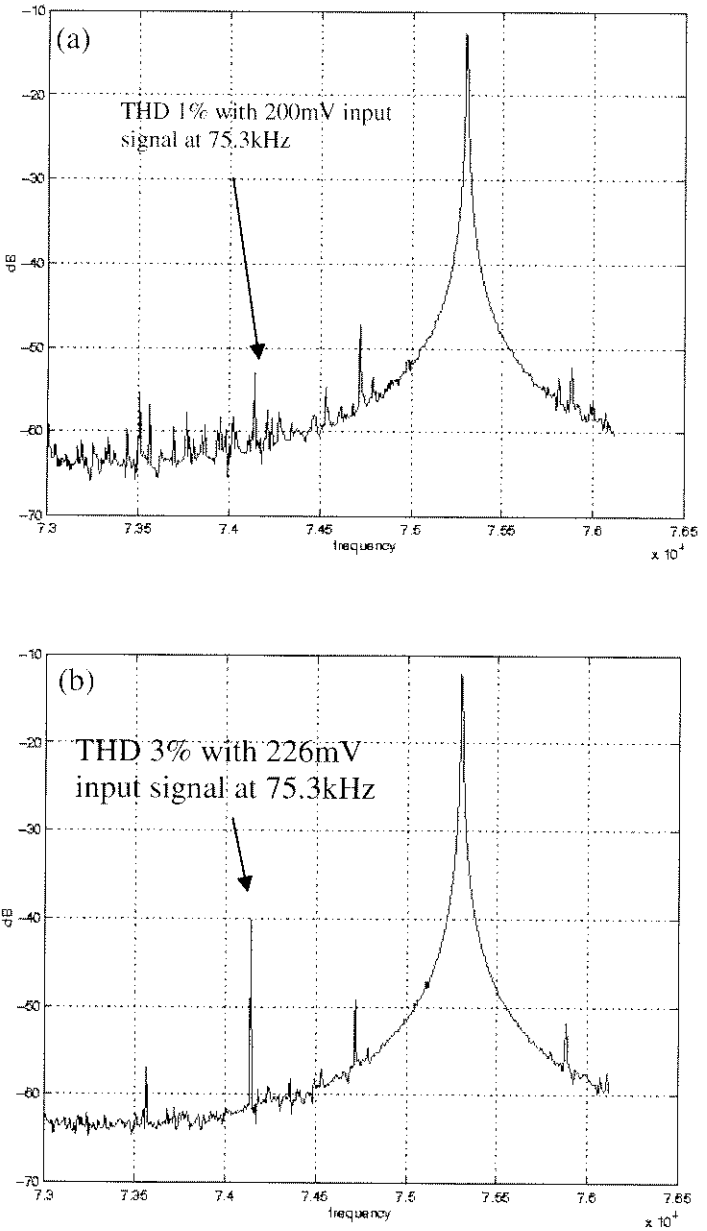


Figure 5.14 Measurement of Total Harmonic Distortion (a) 1% THD (b) 3% THD

Table 5.5 Summary of Filter Performance

Technology	0.5-μm CMOS
Supply Voltage	1 V
Center Frequency	75 kHz
Q Value	45
Sampling Frequency	300 kHz
Max. Output Swing	1.4 V_{pp}
Total Output Noise	1 mVrms
THD 1%	416 mV_{pp}
THD 3%	452 mV_{pp}
Dynamic Range (for 3% THD)	54 dB
Power Consumption	310 μW
Filter Chip Area	0.8 mm^2

The filter is also tested with a single 0.9-V voltage supply. The transient differential output response with a 75-kHz 0.3-V_{pp} input signal is shown in Fig. 5.15, from which the filter is still observed to settle correctly. Figure 5.16 shows the frequency response of the filter for a single 0.9-V supply, which is quite similar to the one measured with a 1-V supply.

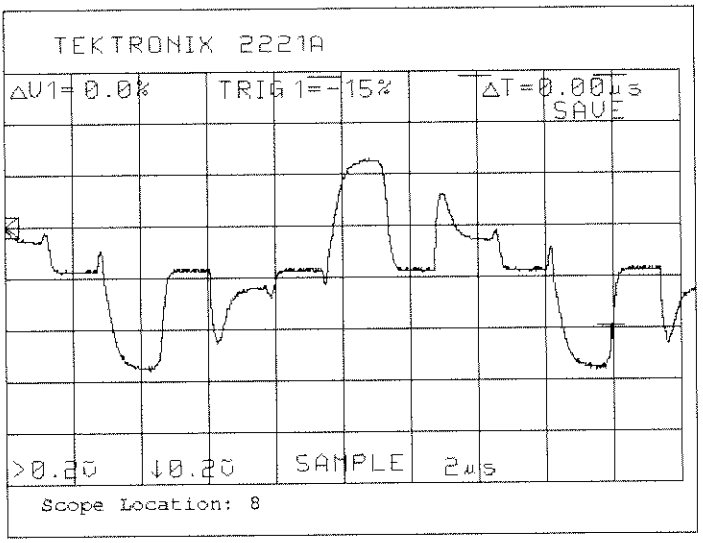


Figure 5.15 Output Transient with 75-kHz 0.3-Vpp Input Signal Using 0.9-V Supply

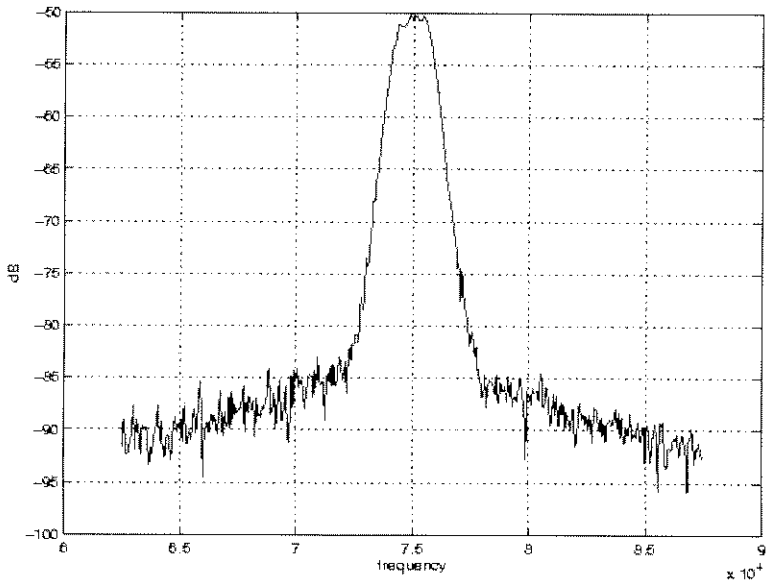


Figure 5.16 Filter Frequency Response at 0.9-V Supply

5.6 CONCLUSION

A novel multi-phase switched-opamp technique is proposed. By using a fully-differential two-switchable-output-pair opamp, the output signal is available in any clock cycle, and hence useful SC techniques like pseudo-N-path can be implemented at low supply voltages. The idea is illustrated through the design and implementation of a 1-V SC pseudo-2-path filter using the proposed switched-opamp technique in a 0.5-μm standard CMOS process. The opamp has a measured low-frequency gain of 69 dB with a phase margin of 45°. With a sampling frequency of 300 kHz, the filter achieves a passband bandwidth of 1.7 kHz at center frequency of 75 kHz, which corresponds to a quality factor Q of 45. The 1% THD is measured with in-band input signal amplitude of 0.42 V_{pp}. The filter dissipates a power of 310 μW and occupies a chip area of 0.8 mm^2. Proper operation of the SC pseudo-2-path filter is still observed with supply voltages as low as 0.9 V.

Chapter 6

DESIGN OF LOW-POWER AND HIGH-FREQUENCY SWITCHED-OPAMP CIRCUITS

6.1 Introduction

In 1994, switched-opamp (SO) technique [CRO 94] has been shown to be a promising low-cost solution to realize SC circuits at 1-V in standard CMOS processes. Since then, a few numbers of modifications [BAS 97a, CHE 00b] have been proposed to improve the performance of the switched-opamp technique in terms of operation speed and compatibility with most of the existing SC systems. Yet, SC circuits employing those switched-opamp techniques at 1-V operation can only achieve a reported operation speed up to 10 MHz, which is far lower than the SC circuits at higher voltages. This chapter focuses on the development of switched-opamp circuits, on both system-level and circuit-level, to handle with both low power and high frequency applications. Up to 50 MHz of operation speed was measured through the demonstration of a 1-V 10.7-MHz CMOS switched-opamp bandpass $\Sigma\Delta$ modulator [CHE 02b].

On the system level, the proposed fast-settling double-sampling SC biquadratic filter architecture (Chapter 3 Section 3.3) is employed to achieve high-speed operation. Besides, a low-voltage double-sampling (DS) finite-gain-compensation (FGC) technique [NAG 97] is employed to realize high-resolution $\Sigma\Delta$ modulator using only low-DC-gain opamps to maximize the speed and to reduce power dissipation. On the circuit level, a fast-switching methodology is proposed for the design of the switchable opamps to achieve switching frequency up to 50 MHz. The operation frequency is improved five times more than prior 1-V switched-opamp designs and comparable to the performance of the state-of-the-art SC circuits that operate at much higher supply voltages. Implemented in a 0.35-μm CMOS process (V_{TP} = -0.8 V and V_{TN} = 0.65 V) and at 1-V supply, the modulator achieves a measured peak signal-to-noise-and-distortion-ratio (SNDR) of 42.3 dB at

10.7 MHz with a signal bandwidth of 200 kHz while dissipating 12 mW and occupying a chip area of 1.3 mm^2.

6.2 Bandpass ΣΔ Modulator Topology

Figure 6.1 shows the block diagram of a second-order bandpass ΣΔ modulator topology [BAS 97b, CHE 02b], which consists of an adder, a resonator, a 1-bit analog-to-digital converter and a 1-bit digital-to-analog converter (DAC). The ideal transfer characteristic of the bandpass ΣΔ modulator is given below:

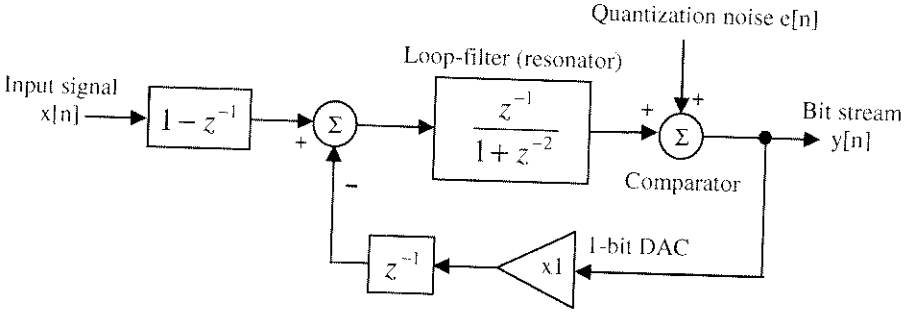


Figure 6.1 Linear Model of a Second-Order Bandpass ΣΔ Modulator

$$Y(z) = z^{-1}(1 - z^{-1})X(z) + (1 + z^{-2})E(z)$$

It can be observed, in the z-domain, that the input signal is shaped with a highpass function $z^{-1}(1\text{-}z^{-1})$ instead of a delay (z^{-2}) as in most ΣΔ modulator bandpass designs [A.AZI 96] while the quantization noise is still shaped with a notch function at the center frequency of the modulator. Similar to conventional second-order bandpass ΣΔ modulators, every doubling of the over-sampling-ratio (OSR) offers a 9-dB improvement in the signal-to-noise-ratio (SNR). Theoretically, the maximum achievable SNR of this ΣΔ modulator is about 60 dB at an OSR of 107. For a bandpass SC ΣΔ modulator, it is possible to use only AC-coupling capacitor (C_G) to realize the highpass function for the input branch of the ΣΔ modulator [BAS 97a]. For low-voltage operation, this is an advantage since the AC-coupling capacitor basically does not impose any swing limit to the input signal. The adder and the DAC can be easily implemented with switching capacitors in SC circuits. The quantizer can be easily realized with a latch-type comparator to save static power consumption. The discrete-time resonator can be easily realized from most of the reported SC biquadratic architectures [FLE 79, GRE 86, ANA 95, KI 95], which are generally insensitive to process variations. Therefore, the modulator performance can be preserved without acquiring automatic tuning circuits [LIN 99], which would generate additional noise

and consume extra power as in continuous-time ΣΔ modulators. Nevertheless, as explained in Chapter 3, the conventional SC biquadratic filters may not be optimal for high-speed applications, the proposed fast-settling double-sampling SC biquadratic filter architecture (Chapter 3, Section 3.3) is employed to implement the resonator for the bandpass ΣΔ modulator.

6.3 Fast-Settling Double-Sampled SC Resonator

Figure 6.2 shows the proposed fast-settling double-sampled SC resonator. The corresponding minimum switch configuration can be easily obtained by combining those switches with same function. The transfer function of the proposed SC resonator architecture is written as shown below:

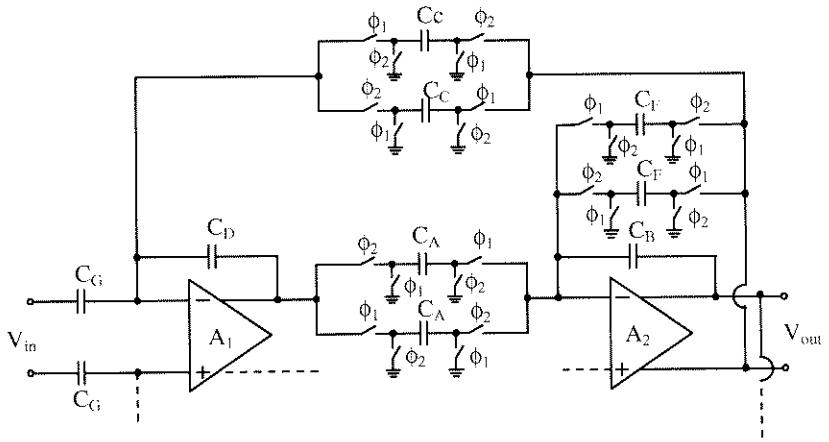


Figure 6.2 Proposed Fast-Settling Double-Sampled SC Resonator

$$H(z)=\frac{V_{out}(z)}{V_{in}(z)}=-\frac{C_A C_G z^{-1}\left(1-z^{-1}\right)}{C_D C_B+\left(C_F C_D-2C_B C_D\right)z^{-1}+\left(C_B C_D+C_A C_C-C_F C_D\right)z^{-2}}$$

Intuitively, by choosing $C_F = 2C_B$, $C_F C_D = C_C C_A$ and $C_A C_G = C_B C_D$, the required resonator for the ΣΔ modulator can be implemented as illustrated below.

$$Assume \quad C_F = 2C_B, C_A C_C = C_F C_D, C_A C_G = C_B C_D$$

$$H(z) = -\frac{z^{-1}\left(1-z^{-1}\right)}{1+z^{-2}}$$

By operating in a double-sampling manner, the unity-gain-frequency requirement of the opamps is reduced by 50%, compared with conventional SC biquadratic filter as explained in previous section. Moreover, unlike the double-sampled SC biquadratic filter in [NAG 97], the proposed architecture employs only non-inverting delay SC integrators for the realization of the core of the filter such that there is no direct feedback in the architecture. As a result, the two opamps are decoupled from each other to achieve independent and fast settling. Besides, the use of non-inventing delay SC integrators is also immune to parasitic effects [GRE 86].

6.4 1-V Double-Sampling Finite-Gain-Compensation Technique

Although opamp bandwidth requirement is reduced by 50% with double-sampling technique, high opamp gain (usually over 60dB) is still required to preserve the resonator performance [A.ANA 95]. As a result, most high-frequency SC ΣΔ modulators consume large power [SON 89, ONG 97, BAZ 98]. To further reduce the opamp gain and bandwidth requirements, finite-opamp-gain compensation technique can be applied. Figure 5.3 illustrates the effect of finite opamp gain to the performance of a SC integrator [MAR 81, GRE 86].

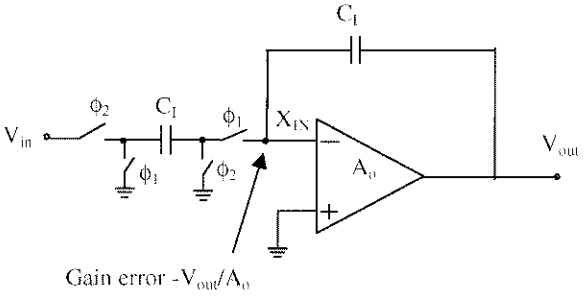


Figure 6.3 Effect of Finite-Gain Opamp in SC Integrator

Obviously, due to finite opamp gain, a residual error is imposed at the input terminal of opamp at every integration event of a SC integrator and thus limits the accuracy. This in turns limits the resolution of the ΣΔ modulator. On the other hand, if the output signal can be effectively predicted, a battery that is pre-charged with the amount of gain error can be used to make the charge transferring node a perfect virtual ground as shown in Fig. 6.4.

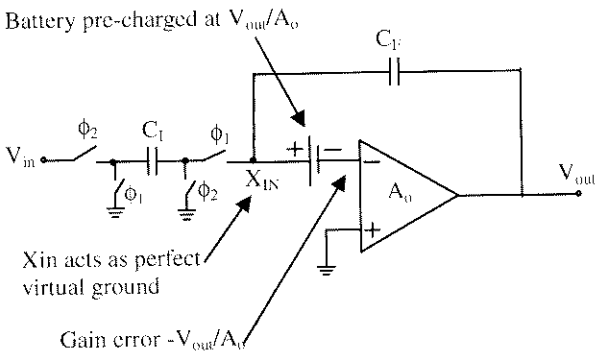


Figure 6.4 Compensated SC Integrator

Theoretically, the opamp DC gain can be compensated to make it infinite with a perfect prediction scheme. In practice, a few number of possible compensation techniques have been proposed [KI 91, 95, NAG 97] in recent years to significantly reduce the finite-opamp-gain error to achieve good circuit performances. Specifically, for bandpass applications, the double-sampling finite-gain-compensation (DSFGC) technique proposed in [NAG 97] can be employed to achieve a compensated opamp gain up to A_o^2, where A_o is the actual opamp DC gain. The concept of the DSFGC technique [NAG 97] is based on the fact that the output waveform of a high-Q bandpass filter being sampled at f_s is basically a sinusoidal waveform at the filter center frequency f_c. Moreover, if the ratio f_s/f_c is chosen to be equal to 4, the output, as illustrated graphically in Fig. 6.5, will consist of only four samples with magnitudes V_1, V_2, V_3 and V_4, where $V_1 = -V_3$ and $V_2 = -V_4$.

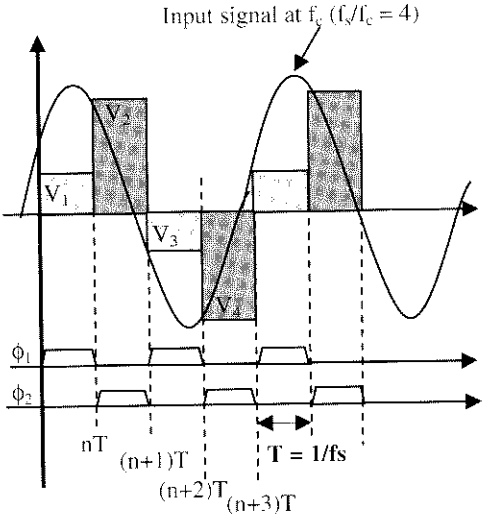


Figure 6.5 Illustration of DSFGC Scheme

In other words, if the output components V_1 and V_2 can be memorized by the system, they can be used to predict and to effectively compensate the gain errors for the next two output components V_3 and V_4. For signals at frequencies other than f_c, the compensation will be less effective as the stored samples cannot be used to accurately predict future samples for compensation. As a result, this technique is most effective for realizing high-Q bandpass filter and is perfectly suitable for implementing the resonator required for the bandpass ΣΔ modulator.

For low-voltage operation with a high-swing output, the DSFGC architecture proposed in [NAG 97] must be modified to avoid connecting MOS switches at the opamp outputs. This is achieved by using the SO technique proposed for multi-phase operation in [CHE 00b] together with the free sign-inversion [INO 86] from a fully-differential architecture. Figure 6.6 shows the proposed low-voltage fully-differential DSFGC SO integrator using the multi-phase SO technique.

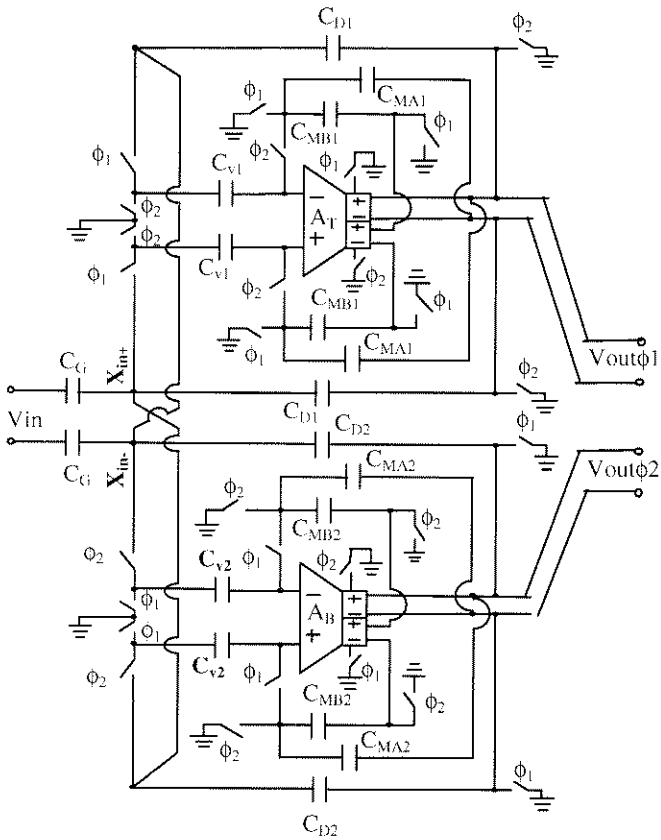


Figure 6.6 Proposed Low-Voltage SO DSFGC Integrator

The proposed DSFGC employs two switchable opamps, each of which has a single differential input stage and two pairs of differential output stages that are turned on and off alternately to implement the multi-phase SO technique [CHE 00b]. The integrator capacitor is realized with two capacitors C_{D1} and C_{D2} of the same size as discussed previously in the multi-phase SO technique. C_{v1} and C_{v2} are the battery capacitors, which compensate for the finite gain error during integration. C_{MA1} and C_{MA2} are the memory capacitors on which the output samples are stored while C_{MB1} and C_{MB2} (having the same size as C_{MA1} and C_{MA2}) are used to achieve the required sign inversion for the gain compensation. At $t = nT$, $\phi_1=1$, opamp A_T operates on the input $V_i[nT]$ and produces the output $V_{out}[nT] = V_1$, which is sampled and stored by C_{MA1}. Gain compensation for input $V_i[(n+2)T]$ can be performed during $t = (n+1)T$ and $\phi2 = 1$, where C_{MB1} is connected to the opamp in feedback loop while C_{MA1} is discharged and with the stored output signal injected into C_{MB1}. As a result, the opamp output voltage is set to about $-V_{out}[nT]$ if $C_{MA1} = C_{MB1}$. Capacitor C_{v1} is therefore pre-charged to about $V_{out}[nT]/A_o$, where A_o is the actual opamp DC gain. This pre-charged value at C_{v1} is approximately equal to $-V_{out}[(n+2)T]/A_o$, which corresponds to the virtual ground error at the opamp's negative input terminal during processing the input signal $V_i[(n+2)T]$. At $t = (n+2)T$, capacitor C_{v1} remains charged at the value previously acquired and acts like a battery in series with the opamp's negative input terminal. Similar operations are carried out by the bottom opamp (A_B) but in opposite phases as A_T. Unlike in conventional double-sampling techniques, however, two opamps are required here for each integrator to implement gain-compensated double sampling. The transfer characteristic of the finite-gain-compensation technique is written as follows:

$$X_{in}^{+}[(n+1)T_c] - X_{in}^{-}[(n+1)T_c] \approx -\frac{V_o^{+}[(n+1)T_c] - V_o^{-}[(n+1)T_c]}{A_o^2}$$

The equation shows that the DSFGC SO integrator, with the input terminals X_{in+} and X_{in-} acting as the virtual ground, exhibits an effective opamp gain of A_o^2, where A_o is the actual opamp DC gain. To verify the efficiency of the proposed low-voltage gain-compensation technique, three simulated SC resonator responses are obtained with SWITCAP2 [FAN 83] as shown in Fig. 6.7. Figure 6.7(a) and (b) show two responses of a resonator using the conventional SC biquadratic architecture with opamp gain of 5000 V/V and 70 V/V respectively. Obviously, not only the peak of the resonator drops significantly, but also the center frequency shifts in case of an insufficient opamp gain. On the other hand, as illustrated in Fig. 6.7(c), even with an opamp gain of only 70 V/V, SC resonator that employs the DSFGC technique can still have its response well preserved as if a conventional SC resonator using high opamp gain. Though the passband and center frequency characteristics of a resonator are maintained with the employment of DSFGC

technique, the resultant stopband attenuation is even larger than both conventional cases (a) and (b). This is because the DSFGC scheme is designed only to be effective to predict and compensate for errors due to finite-opamp-gain for signals near ¼ of the sampling frequency. As a result, the DSFGC would create more errors to signals that are located far away from ¼ of the sampling frequency. Nevertheless, the effect of the errors created due to incorrect gain-error compensation to signals at the stopband is generally not important to the overall system performance, and in most cases extra stopband attenuation could be a benefit.

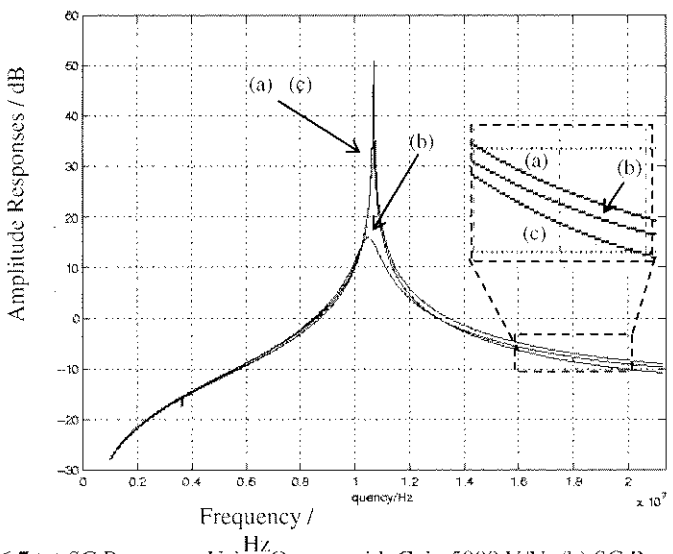


Figure 6.7 (a) SC Resonator Using Opamp with Gain 5000 V/V; (b) SC Resonator Using Opamp with Gain 70 V/V; (c) DSFGC SC Resonator Using Opamp with Gain of 70 V/V

Consequently, by employing the DSFGC technique to implement SC system, the opamp gain requirement is greatly reduced. Moreover, due to the double-sampling feature, the required opamp unity-gain bandwidth is also halved. Hence, the power consumption of the SC system can also be significantly reduced.

6.5 Realization of DSFGC Bandpass ΣΔ Modulator

Figure 6.8 shows the overall implementation of the proposed SO DSFGC ΣΔ modulator. The resonator, which is realized with the proposed fast-settling biquadratic filter architecture, consists of two DSFGC integrators as described in previous sections with capacitive input coupling (C_G) to achieve large input signal swing at low-voltage. This would provide unlimited input swing to the modulator at a low-supply voltage.

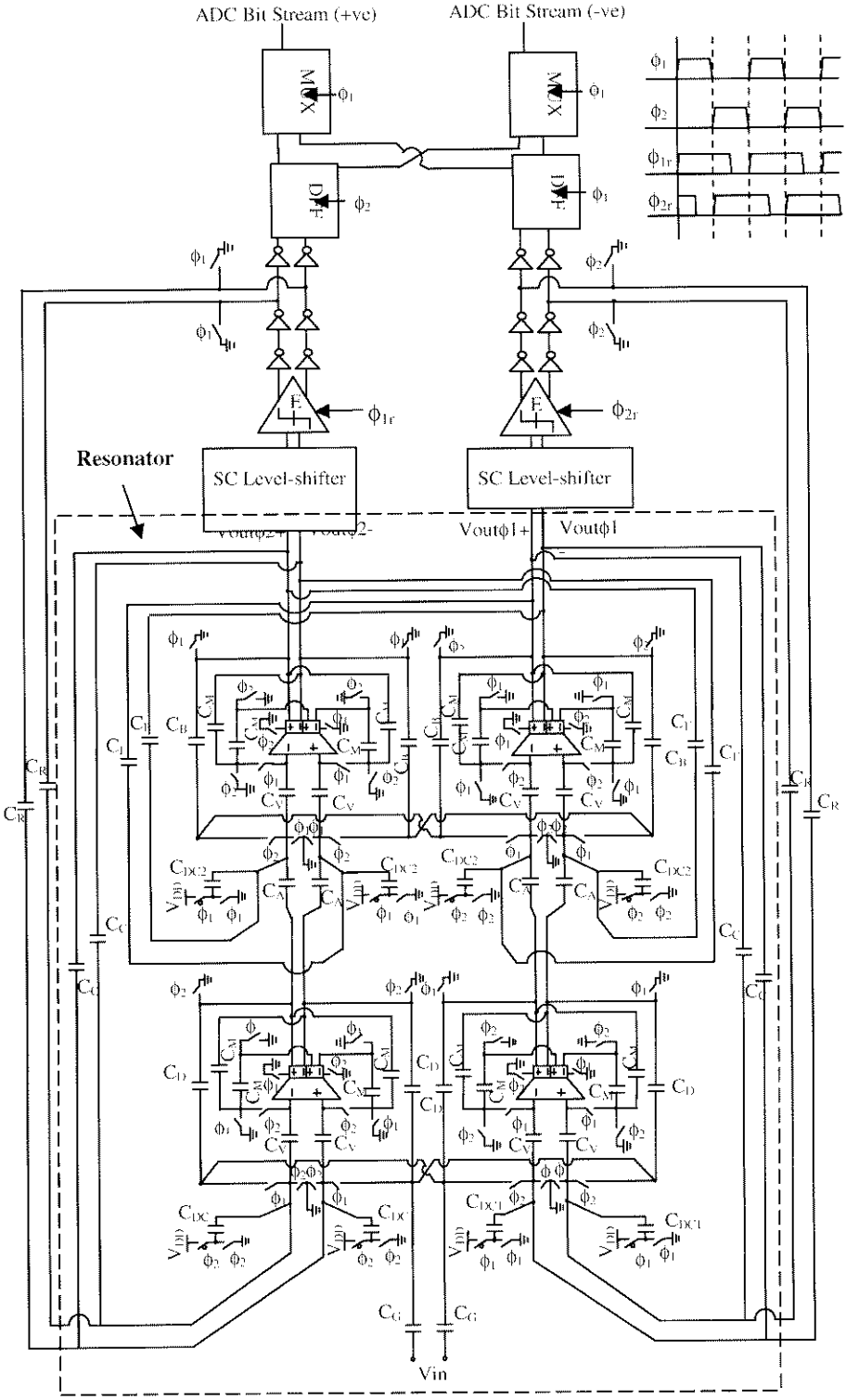


Figure 6.8 Schematic of the Proposed ΣΔ Modulator

Differential latch-type comparators E_1 and E_2 are used to process the resonator outputs at ϕ_1 and ϕ_2 respectively. Clock phases ϕ_{1r} and ϕ_{2r} are applied to reset the comparators E_1 and E_2 respectively before they perform the comparison. The comparator outputs are stored and fed back to the resonator with switched capacitors C_R, which form non-inverting delay SC branches. The comparator outputs are held by two D flip-flops (DFF) and combined at two complementary clock phases using multiplexers (MUX) to produce the output bit streams. The modulator coefficients are optimized with simulations for maximizing the achievable signal-to-noise ratio. Table 6.1 summarizes the value of the capacitors.

Table 6.1 Summary of Capacitor Values

C_A	0.675pF	C_G	0.225pF
C_B	0.405pF	C_R	0.225pF
C_C	0.81pF	C_V	2pF
C_D	0.675pF	C_{M1}	1pF
C_F	0.81pF	C_{M2}	1pF
$C_{DC1} = 0.4C_C + 0.5C_R$		0.436pF	
$C_{DC2} = 0.4C_A + 0.4C_F$		0.594pF	

6.6 Design of Low-Voltage Building Blocks

6.6.1 Current-Mirror Operational Amplifier

As explained in Chapter 4 (section 4.1), primarily due to the long turn-on time of the required switchable opamps, the maximum sampling frequency of switched-opamp circuits is still limited to only a few MHz. Since the switchable opamp is basically operated in slew-limiting situation during the turn-on moment, enhancing its slew-rate performance can significantly reduce its turn-on time. By far, current-mirror opamp topology [JOH 96] has been well known for its excellent slew-rate performance. The reasons are two-folded: Firstly, unlike two-stage opamp topology, current-mirror opamp does not require compensation capacitors that usually limit the opamp slew-rate for a given power consumption. Secondly, the slew-rate performance can be enhanced significantly by scaling the current-mirror ratio in the current-mirror opamp. Figure 6.9 shows the topology of a current-mirror opamp. The detailed analysis of the current-mirror opamp is shown in Table 6.2.

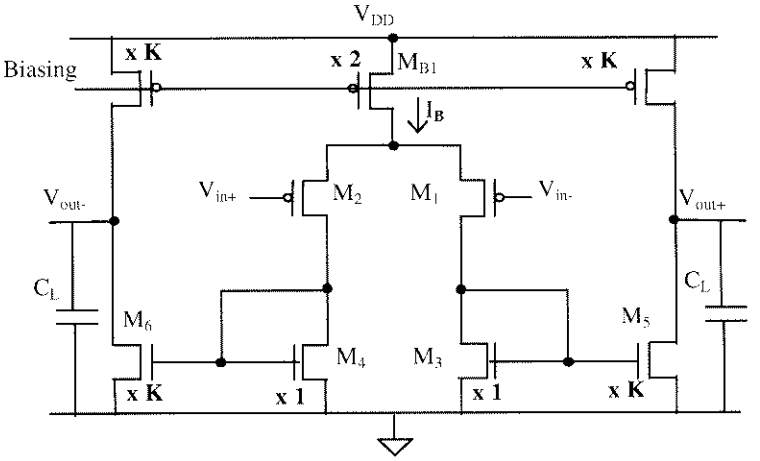


Figure 6.9 Current-Mirror Operational Amplifier

Table 6.2 Summary of Current-Mirror Opamp Transfer Characteristics

Transfer Function

$$\frac{V_{out}}{V_{in}} \approx \frac{-gm_1 gm_5 r_{o5}\left(1-\frac{sC_{gd1}}{gm_1}\right)\left(1-\frac{sC_{gd5}}{gm_5}\right)}{gm_3\left[1-sC_L r_{o5}+s^2\frac{C_L r_{o5}(1+K)C_{gs3}}{gm_3}\right]}$$

where

$$gm_5 = Kgm_3 \quad \textit{and} \quad R_{out} \approx r_{o5}$$

DC Gain

$$A_o \approx -Kgm_1 r_{o5}$$

Slew Rate

$$SR \approx \frac{KI_B}{C_L}$$

Dominant Pole

$$\varpi_{P1} = \frac{1}{R_{out}C_L} \approx \frac{1}{r_{o5}C_L}$$

Second Pole

$$\varpi_{P2} \approx \frac{gm_3}{(1+K)C_{gs3}} = \frac{3\mu_n(V_{GS}-V_T)}{2(1+K)L_{eff}^2}$$

The overall transfer function of the current-mirror opamp is basically a two-pole system with approximately a single-stage-amplifier low-frequency gain. In fact, for high-voltage operation, cascoded output stage can also be employed to improve the overall opamp low-frequency gain to be comparable to that of the two-stage opamps. However, it will severely reduce the output swing of the opamp for low-voltage operation. Besides, as discussed previously, non-cascoded single-stage amplifiers can already achieve sufficient gain for preserving the performance of the proposed ΣΔ modulator with the DSFGC topology.

In Fig. 6.9 and Table 6.2, the K factor is the ratio of the current mirrors, which sets the amount of current amplification from the input stage to the output. Employing a larger K value could improve both the opamp gain and slew-rate, however, the second pole of the opamp also moves to a lower frequency and thus degrades the stability of the opamp. It is worth to mention that the transconductance of the transistors M_3 and M_5 of the current-mirrors to the first order does not affect the opamp DC gain and the bandwidth. Instead, given a current consumption, the design of transistors M_3 and M_5 with a larger gate-to-source-voltage (V_{GS}) can push the second pole farther apart from the dominant pole to obtain better stability performance. This is intuitively true since the transconductance is proportional to the square root of while the parasitic gate-capacitance (C_{GS}) is linearly dependent to the device aspect ratio (W/L). In addition, employing an advanced CMOS process with higher device mobility and smaller device feature size (L_{eff}) could put the second pole location to higher frequency due to the improvement of transconductance and reduction of parasitic capacitance. In fact, for 1-V operation, the V_{GS} of transistors M_3 (M_4) and M_5 (M_6) is limited to a maximum value of about 0.7 V in order to keep the PMOS input transistors M_1 and M_2 and the current source M_{B1} in saturation region. To compromise between the slew-rate and the stability, a moderate K value of 1.67 is used.

6.6.2 1-V Switchable Current-Mirror Opamp with Dual Time-Multiplexed Output Stages

As discussed above, though slew-rate-enhanced opamp topology could reduce the switching time of switchable opamp, the amount of speed improvement is limited by low supply voltages. A new switching mechanism is therefore proposed to further reduce the turn-on time for low supply voltages. Figure 6.10 shows the proposed fast-switching fully-differential opamp with dual time-multiplexed output stages.

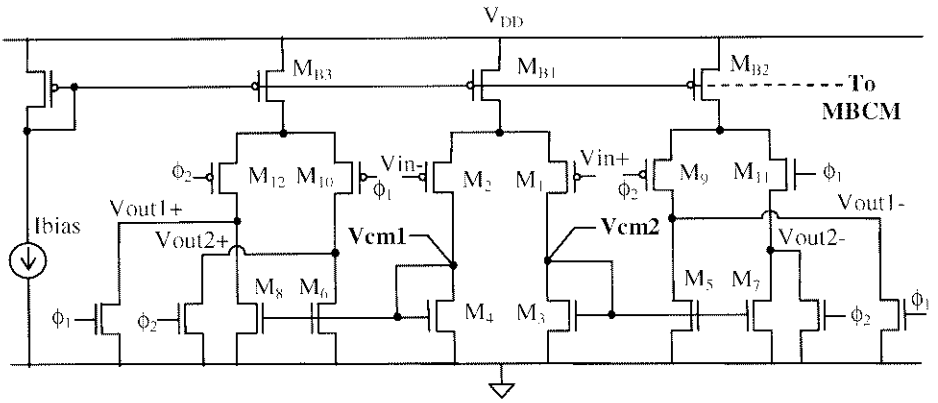


Figure 6.10 Fast-Switching Current-Mirror Opamp with Dual Time-Multiplexed Output Stages

The input stage of the proposed opamp is made up of a PMOS differential-pair (M_1 to M_4) with the common-mode input voltage set at ground. The two identical output stages are controlled to turn on and off alternately using the differential switches M_9 and M_{13} (M_{10} and M_{14}) with a pair of complementary clock phases (ϕ_1 and ϕ_2). Fast turn-on time is achieved not only because the current biases M_{B2} and M_{B3} of the output stages are always kept active but also because the differential switches provide low output impedance at the turn-on instance and thus reduce dramatically the RC time constant associated at the opamp output node. For fast turn-off, additional NMOS switches are added at the outputs to pull them to ground. With all these design techniques, a maximum sampling frequency up to 50 MHz at 1-V supply is measured, which is improved more than ten times compared with prior arts [CRO 94, BAS 97b, WAL 01]. The opamp achieves a measured DC gain of 70 V/V and a unity-gain frequency of 100 MHz for a 3-pF loading at 1-V supply. As a result, the DSFGC topology could provide a compensated and effective opamp gain of 4900 V/V to preserve the performance of the $\Sigma\Delta$ modulator. To maximize the output swing of the opamp, the common-mode output voltage was measured to be 0.4 V with a measured linear output swing of about 0.4 V. Table 6.3 and Table 6.4 summarize the size of the devices used for the opamp and the measured opamp performances respectively.

Table 6.3 Summary of Device Size

Transistors	Unit Size	Quantity
M_{B1}	80μm / 0.8μm	x48
M_{B2}, M_{B3}	80μm / 0.8μm	x40
M_1, M_2	20μm / 0.4μm	x24
M_3, M_4	10μm / 0.6μm	x24
M_5, M_6, M_7, M_8	10μm / 0.6μm	x40
M_9, M_{10}, M_{11}, M_{12}	20μm / 0.4μm	x40

Table 6.4 Summary of Measured Performance of the Proposed Switchable Opamp

Technology	0.35-μm CMOS
Supply Voltage	1 V
Low-Frequency Gain	70 V/V
Unity-Gain Frequency	100 MHz
Phase Margin	50°
Max. Switching Frequency	50 MHz
Power Consumption	2.8 mW
Linear Output Swing (Single-ended)	0.4 V
Loading Capacitor	3 pF
Chip Area	400 x 300 μm^2

6.6.3 Current-Injected Common-Mode Feedback Circuit

Figure 6.11 shows the current-injected error-amplifier-based common-mode feedback circuit (CMFB) for the proposed opamp.

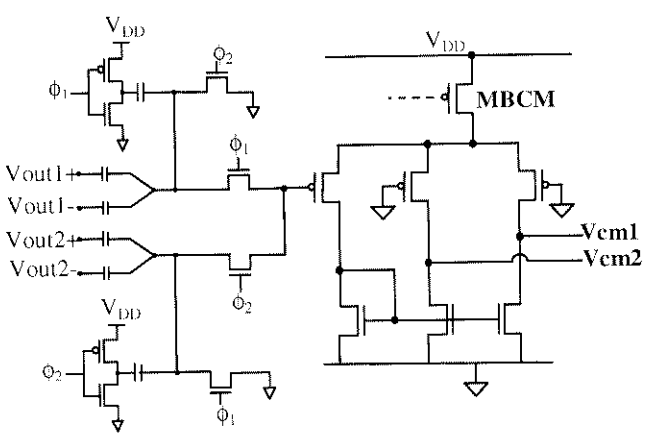


Figure 6.11 Common-Mode Feedback Circuit for the Proposed Switchable Opamp

The CMFB circuit consists of SC level shifters and an error amplifier [WAL 99]. The SC level shifters not only solve the DC-biasing problem between the opamp output nodes and the error-amplifier input but also provide the reference voltage to the CMFB circuit to control the opamp common-mode output voltage to 0.4 V to maximize the opamp's output swing. The proposed current-injected error amplifier, being made of a differential pair with two identical output branches, is employed to enhance the common-mode feedback loop-gain for fast response. The outputs V_{cm1} and V_{cm2} of the CMFB circuit are connected to the current-mirroring nodes of the opamp input stage, which are at low impedance. As a result, error signals that are generated by the SC level-shifters due to inaccurate common-mode output voltage of the opamp will be injected to the error-amplifier and fed back in form of current to the input stage of the opamp at V_{cm1} and V_{cm2} to control the common-mode voltage.

6.6.4 1-V Latch-Type Comparator

The schematic of the 1-V latch-type comparator [PEL 97a] with NMOS regenerative pair is shown in Fig. 6.12.

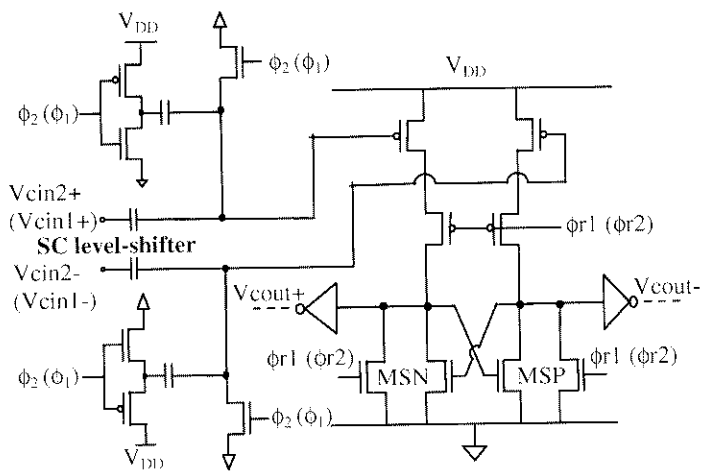


Figure 6.12 1-V Latch-Type Comparator

Similar to the CMFB circuit, SC level-shifters are used not only to generate appropriate bias for the opamp output nodes and the comparator's input nodes but also to provide appropriate reference level for the comparator. The comparator is reset by cutting off M_{C1} and M_{C2} and pulling M_{SN} and M_{SP} to ground at ϕ_{r1}. When ϕ_1 and ϕ_{r1} are high, the comparator is still in the reset

phase, and the SC level shifters pass the differential output signals of the resonator to the input terminals of the comparator. When ϕ_{r1} is low, the comparator makes decision and produces the result. Parenthesized clock phases are used for comparator reset at ϕ_{r2}.

6.6.5 1-V D-Flip-Flop

Figure 6.13 shows the 1-V D-flip-flop (DFF) used for the realization of the ΣΔ modulator.

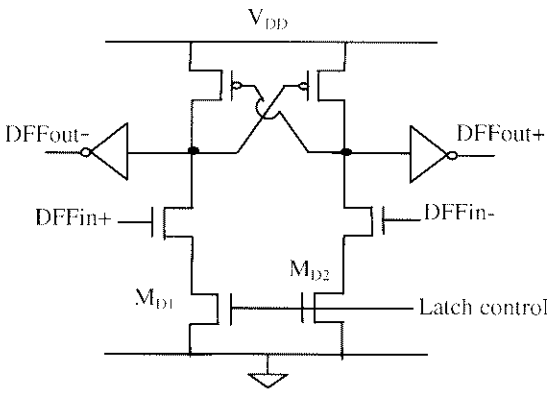


Figure 6.13 1-V D-Flip-Flop

The DFF consists of a PMOS regenerative pair for fast operation. Since the transistors M_{D1} and M_{D2} operates in triode region as switches, the minimum supply voltage is given by $V_{DD} = V_{TP} + V_{satn} \approx 1V$. The DFF latches the result when the latch control goes low such that M_{D1} and M_{D2} are cut off.

6.7 Experimental Results

Figure 6.14 shows the chip photograph of the proposed second-order SO ΣΔ modulator.

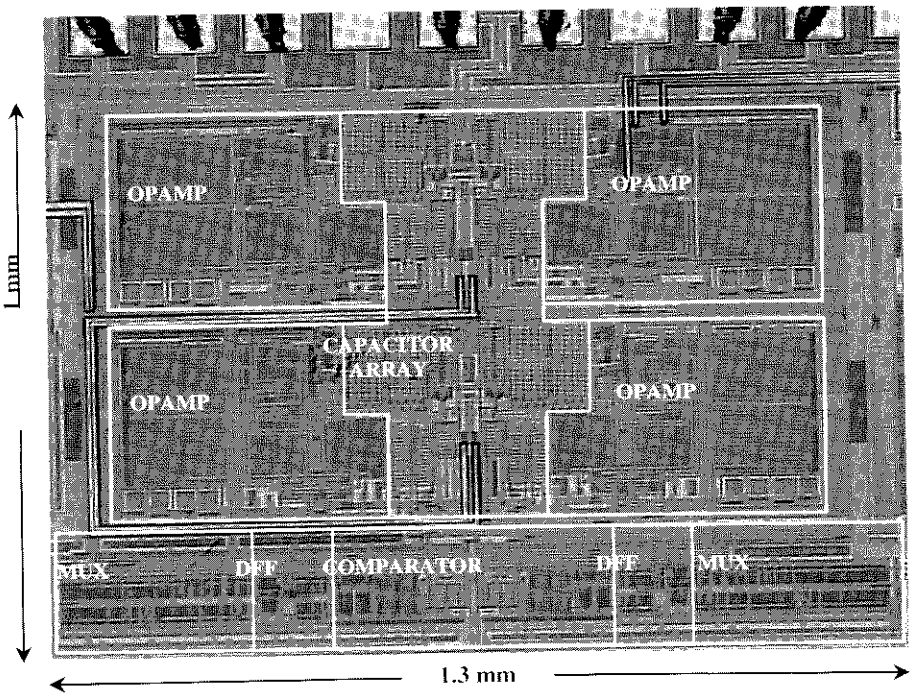


Figure 6.14 Chip Photograph of the Proposed ΣΔ Modulator

The SO ΣΔ modulator is designed and fabricated in a standard double-poly four-metal 0.35-μm CMOS process (V_{TP} = -0.8 V and V_{TN} = 0.65 V). The chip area is about 1.3 mm^2. Poly-to-poly capacitors are used for good linearity. The opamps are distributed evenly at two sides while all capacitors are laid out close together for good matching. The analog circuits (opamps and switched-capacitors) are placed at the top surrounded by a guard ring to minimize the switching noise coupling from the digital parts (comparators, DFFs and multiplexers), which are placed at the bottom of the layout.

Figure 6.15(a) plots the measured output frequency spectrum of the ΣΔ modulator operated at 1-V supply with an input frequency of f_{in} = 10.676 MHz. The ΣΔ modulator operates at a clock frequency of 21.4 MHz to achieve an effective sampling frequency of 42.8 MHz with the double-sampling technique. The bandpass noise-shaping function is accurately centred at 10.7 MHz as designed, which verifies that the proposed SO

DSFGC scheme indeed achieves high effective opamp gain and preserves the resonator performance.

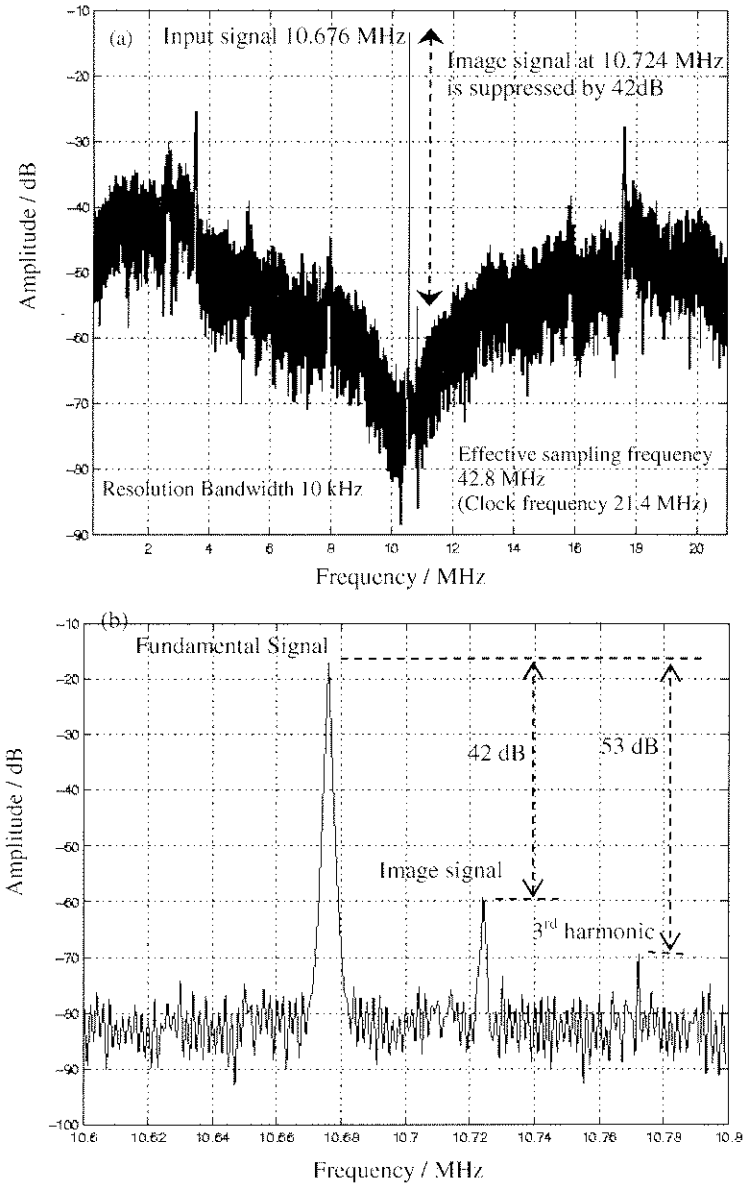


Figure 6.15 (a) Measured Output Frequency Spectrum of the Proposed ΣΔ Modulator at 42.8 MHz Operation; (b) Expanded View of the Output Spectrum

Figure 6.15(b) plots the zoom-in frequency spectrum with a –17-dBV 10.676-MHz input signal at which the peak SNDR is obtained. The image signal created coherently with the double-sampling structure [BAZ 98] is located at $f_s/2 - f_{in}$ = 10.724 MHz and is suppressed by 42 dB which is considerably better than the image-rejection requirements by many applications [BLU 99]. A 42-dB image suppression is equivalent to a path matching as good as 0.1%. The third-harmonic component of the input signal is located at $3*f_{in}$ = 32.028 MHz and folded back at $f_s - 3*f_{in}$ = 10.772 MHz, which is inside the interested 200-kHz bandwidth centered at 10.7 MHz, and is measured to be 53 dB below the fundamental. Figure 6.16 plots the SNDR as a function of the input level.

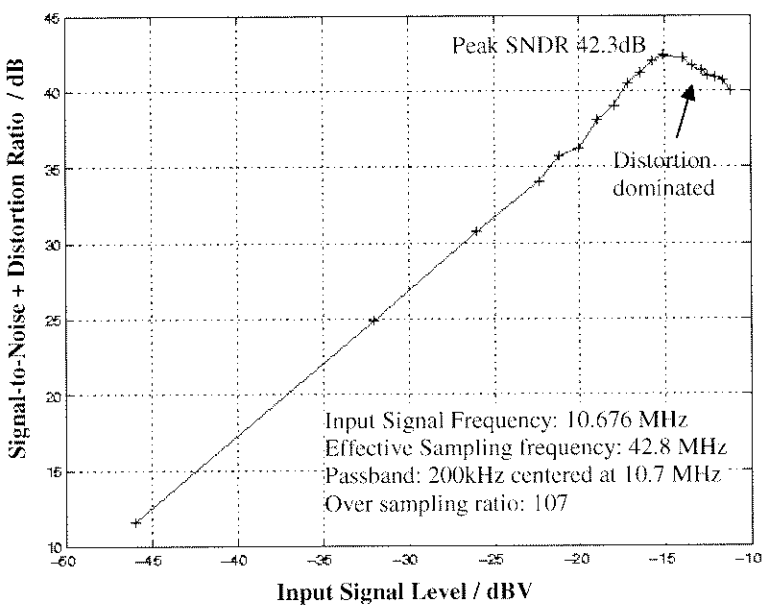
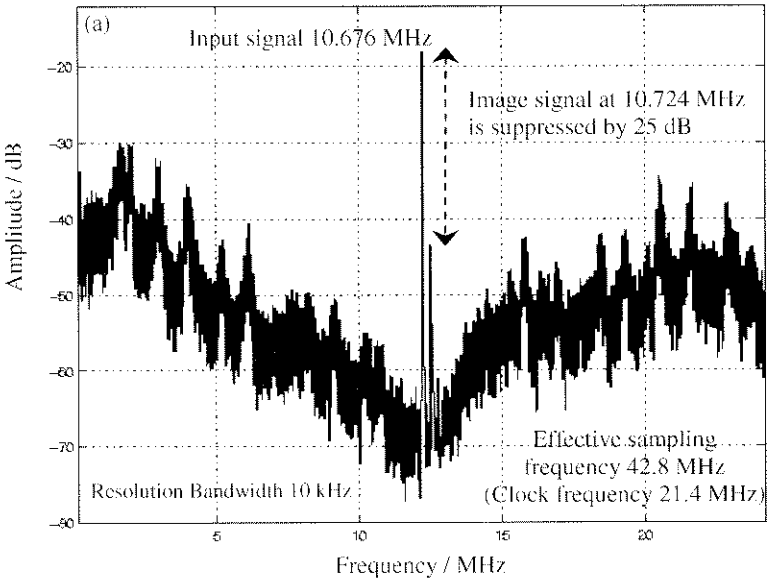


Figure 6.16 Measured SNDR vs. Input Signal Level

The SNDR is measured from the frequency spectrum captured through a spectrum analyzer. Unfortunately, the capturing system does not have an averaging property and so resulting in noise fluctuation during capturing. As a result, though the slope of the measured SNDR versus input signal level is very close to one, it does not has a slope of unity. The measured peak SNDR is 42.3 dB (not including the image signal) with a bandwidth of 200 kHz at an input level of –15 dBV. At 1-V operation, the ΣΔ modulator dissipates 12 mW.

Theoretically, with a bandwidth of 200 kHz and a sampling frequency of 42.8 MHz, the over-sampling-ratio (OSR) is about 107, and the maximum achievable SNR of this second-order bandpass ΣΔ modulator is about 60 dB. Hspice simulation result shows an achievable peak SNDR of 49.5 dB with an input magnitude of –10 dBV. The difference between calculation and simulation could be caused by several factors, namely the non-linear behaviours of the ΣΔ modulator and the non-idealities of the circuit performance. The measurement result is 7 dB lower than the simulation result mainly due to the significant increase in harmonic distortion at input magnitude larger than –15 dBV. The distortion is caused by insufficient settling time and unexpected reduction of linear output swing of opamp from 0.5 V to 0.4 V. To verify the settling problem, the ΣΔ modulator is tested at a sampling frequency of 21.4 MHz. With the same OSR, a peak SNDR of 46 dB is achieved with an input magnitude of –12 dBV. Nevertheless, because of the reduction of the opamp output swing, large distortion is resulted with input levels larger than –12 dBV and thus reduces the maximum achievable peak SNDR. For sampling frequencies below 20 MHz with the same OSR, peak SNDR measurements of about 46 dB are obtained. This shows that the settling error is dominant at sampling frequencies above the designed value, which is 42.8MHz.

The ΣΔ modulator is also measured at a sampling frequency up to 50 MHz. Figure 6.17(a) shows the measured frequency spectrum with a 12.475-MHz input signal at a sampling frequency of 50 MHz. A proper operation is still observed but the performance is poorer mainly due to insufficient settling time.



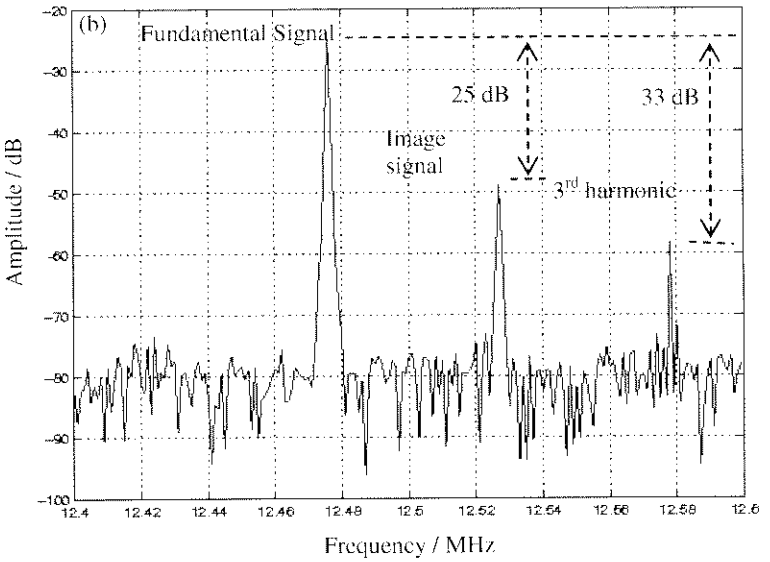


Figure 6.17 (a) Measured Output Frequency Spectrum of the Proposed ΣΔ Modulator at 50 MHz Operation; (b) Expanded View of the Output Spectrum

Figure 6.17(b) plots the zoom-in spectrum with a –20-dBV 12.475-MHz input signal at which the peak SNDR is measured. The image located at a frequency of $f_s/2 - f_{in}$ = 12.525 MHz is suppressed by 25 dB. The third-harmonic component located at $3*f_{in}$ = 37.425 MHz and folded back at $f_s - 3*f_{in}$ = 12.575 MHz is measured to be 33 dB below the fundamental. At an input level of –20 dBV, the modulator achieves a peak SNDR of 25 dB (not including the image).

Table 6.5 summarizes the performance of the proposed ΣΔ modulator together with that of other modulators. Compared to the switched-opamp ΣΔ modulator designs in [PEL 98a, BAS 97b], the proposed SO DS FGC ΣΔ modulator achieves a sampling frequency at least ten times higher and a comparable SNDR while operating at similar supply voltages at a cost of consuming more power. In comparison to the 5-V BiCMOS switched-capacitor ΣΔ modulator designs in [F.SIN95, FRA 96], not only does our modulator operate at much lower supply voltage (1 V) but it also consumes much less power while achieving acceptable SNDR.

Table 6.5 Performance Summary of the Proposed DSFGC ΣΔ Modulator and State-of-the-Art ΣΔ Modulators

Design	[CHE 02b]	[V.PEL 98a]	[BAS 97b]	[SIN 95]	[FRA 96]
Technique	Switched-Opamp			Switched-Capacitor	
Technology	0.35-μm CMOS	0.5-μm CMOS	0.5-μm CMOS	0.8-μm BiCMOS	1.2-μm BiCMOS
Voltage	1 V	0.9 V	1 V	5 V	5 V
Sampling Frequency	42.8 MHz	1.538 MHz	1.8 MHz	42.8 MHz	42.8 MHz
Center Frequency	10.7 MHz	NA	400 kHz	10.7 MHz	10.7 MHz
Bandwidth	200 kHz	16 kHz	20 kHz	200 kHz	200 kHz
Order	Second	Third	Second	Second	Second
Type	Bandpass	Lowpass	Bandpass	Bandpass	Bandpass
Peak SNDR	42.3 dB	62 dB	42 dB (SNR)	57 dB (SNR)	46 dB (SNR)
Chip Area	1.3 mm^2	0.85 mm^2	1.5 mm^2	NA	0.84 mm^2
Power	12 mW	40 μW	240 μW	60 mW	30 mW

6.8 Conclusion

A 1-V ΣΔ modulator is presented using a high-speed SO technique to achieve a sampling frequency of up to 50 MHz, which is improved about five times compared to prior switched-opamp designs and comparable to the performance of the state-of-the-art SC circuits that operate at much higher supply voltages. A low-voltage DS FGC technique is proposed to realize high-resolution ΣΔ modulator using only single-stage low-gain high-bandwidth opamps to maximize the speed and to reduce power dissipation. In addition, a fast-switching methodology is also proposed for the design of the switchable opamps to achieve switching frequency up to 50 MHz. An error-amplifier-based CMFB is embedded in the opamp for optimal operation. At 1-V, the modulator achieves a measured peak SNDR of 42.3 dB at 10.7 MHz with a signal bandwidth of 200 kHz.

Chapter 7

DESIGN OF LOW-POWER AND HIGH-LEVEL-INTEGRATED SWITCHED-OPAMP CIRCUITS

7.1 Introduction

Nowadays IC designers are constantly challenged not only with single-chip integration but also with low-voltage and low-power designs. This is motivated both by the increasing demand of low-voltage low-power IC designs from most market segments and by the reliability concern under voltage scaling of deep-submicron CMOS processes. While many low-voltage RF circuits [SHA 97, WAN 98, WON 02] have been able to operate at very low supply voltages, and recently low-voltage receiver front-end [UGA 01] has been demonstrated with special SIMOX/CMOS processes of low V_T, the possibility of integrating 1-V channel-select filter and A/D converter in a CMOS process with high-V_T is still unknown.

Implemented in a standard 0.35-μm CMOS technology, simulation results of a 1-V analog front-end circuit for Bluetooth receiver applications have been shown possible and recently published [CHA 01]. With the availability of the 1-V CMOS quadrature IF circuitry, a monolithic Bluetooth receiver can be realized using only single 1-V supply to reduce power dissipation and thus the life of batteries for portable applications. Monolithic implementation also reduces the cost as well as the size and weight of the portable equipment. In this chapter, the realization of 1-V quadrature IF-filter and quadrature ΣΔ modulator is presented. Using the switched-opamp technique, the integration of the low-voltage quadrature IF circuitry for Bluetooth receivers is demonstrated in a standard 0.35-μm CMOS process.

7.2 System Description

Figure 7.1 shows the simplified block diagram of the proposed Bluetooth receiver, which consists of a low-noise amplifier (LNA), image-rejection mixers, anti-aliasing filters, frequency synthesizer and quadrature IF circuitry for channel selection and A-to-D conversion. Table 7.1 summarizes the key specifications [BLU 99] of the wireless receiver for Bluetooth applications.

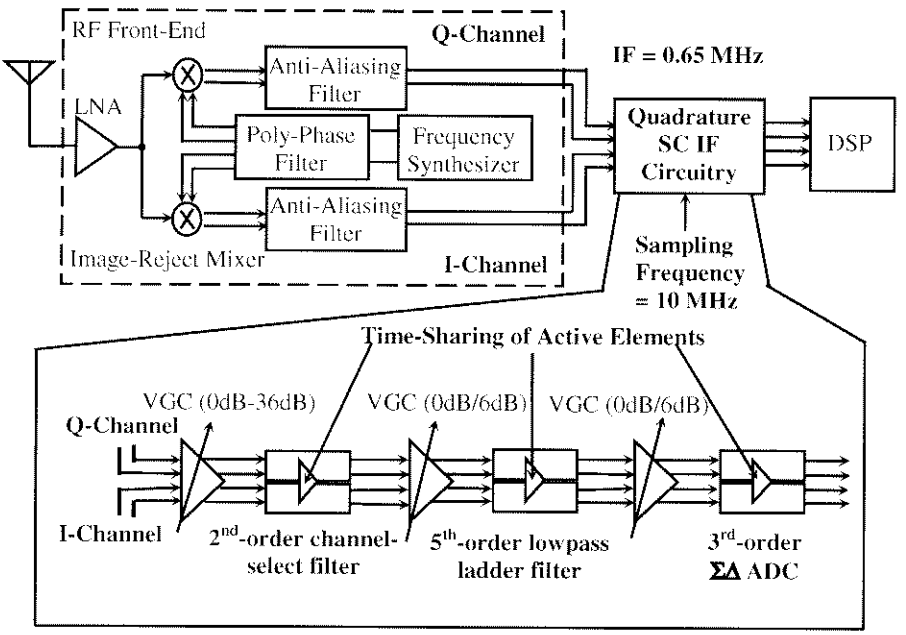


Figure 7.1 Single-IF Bluetooth Receiver Architecture Using Proposed Quadrature IF-Filter and ΣΔ Modulator

Table 7.1 Summary of Key Specifications of the Proposed Bluetooth Receiver

Key Specifications	
Frequency Band	2.4 - 2.48GHz
Sensitivity @ 0.1% Bit Error Rate (BER)	< -70 dBm
Image Rejection	> 20 dB
Noise Figure	< 22 dB
Linearity	> -16 dBm
Channel Spacing	1 MHz
Bandwidth / Data-Rate	1 MHz
VCO Phase Noise	< 89 dBc
Modulation	GFSK
Additional Design Parameters	
Technology	0.35-µm CMOS
Supply Voltage	1 V
Total Power Consumption	< 50 mW
Intermediate Frequency	0.65 MHz
Variable Gain Control	48 dB
Output Signal-to-Noise Ratio	> 9 dB

Antenna receives radio-frequency (RF) signals to pass to the low-noise amplifier (LNA) for amplification of the interested signal band of 2.4 GHz to 2.48 GHz. According to the specifications of the Bluetooth system [BLU 99], a 20 dB in-band image rejection is required, which usually can be easily achieved by employing image-rejection mixer provided that good I-Q VCO signals are available. Good layout techniques should also be employed to keep good matching between the two mixers in order to maintain sufficient image-rejection. Since the image-rejection requirement is not high, a single-conversion super-heterodyne architecture [RAZ 98, BEH 00] with a low intermediate frequency (IF) of 0.65 MHz can be chosen to minimize the power dissipation compared using a high-IF receiver [GUO 01] or dual-conversion [TAD 01] topology, while coherently avoiding DC-offset and Flicker noise problems that occurs in direct-down systems [RAZ 97]. To operate the quadrature switched-capacitor IF circuitry at low power consumption, a low sampling frequency of 10 MHz is used. A minimum of 30-dB rejection to aliasing signals at 9.35 MHz is achieved by employing a third-order lowpass anti-aliasing filter with cut-off frequency at around 1.6 MHz. The quadrature IF circuitry [CHE 03b] consists of a quadrature seventh-order IF-filter (a cascade of a second-order biquadratic SC bandpass filter and a fifth-order ladder lowpass filter to achieve a 1-MHz bandwidth at a center frequency of 0.65 MHz) and a third-order lowpass $\Sigma\Delta$ modulator with extended noise-shaping to obtain at least 12-dB signal-to-noise-ratio. Variable-gain-control (VGC) stages are inserted between these blocks to achieve a total gain control of 48 dB. The quadrature outputs are combined in the digital domain through digital-signal-processing (DSP) where decoding of signals is carried out. Therefore, DSP technique can also be employed to further improve the image-rejection.

To address the low power dissipation requirement of the Bluetooth receiver, new design techniques at both the system and the circuit levels are proposed. To achieve for the highest power efficiency, the whole quadrature IF circuitry is built using only half-delay switched-capacitor (SC) integrators. As described in Chapter 3 half-delay-SC-integrators-based architectures require the opamp to be active only during the integration phase, which allow up to 50 % power reduction to the whole system. To operate at a single 1-V supply, switched-opamp technique is employed to realize the half-delay-SC-integrator-based biquadratic filter, ladder filter and $\Sigma\Delta$ modulator topologies for the quadrature IF circuitry for Bluetooth receiver. Besides, a deeper insight of the advantage of using half-delay SC integrators for SC system is on the possibility to time-share the active elements among the quadrature channels to enjoy both better channel matching and lower power consumption. In order to achieve it, a novel dual-input switchable opamp is designed to coherently avoid coupling of signals and allow time-sharing of the opamps between the quadrature channels.

7.3 Design of 1-V Switched-Opamp Biquadratic Filter

As mentioned in Chapter 2, switched-opamp technique [CRO 94, CHE 00b] maintains low sensitivity to opamp finite gain while saving 50 % power consumption compared with the SC counterpart when applied to implement the half-delay non-inverting SC integrator. Fig. 7.2 shows the switched-opamp realization of the proposed half-delay-SC-integrator-based biquadratic filter in Chapter 3 for channel-selection. By eliminating those problematic switches and replacing the original opamps with switchable opamps that are set active during their integration phases, a low-voltage SC channel-select filter of the IF circuitry is implemented.

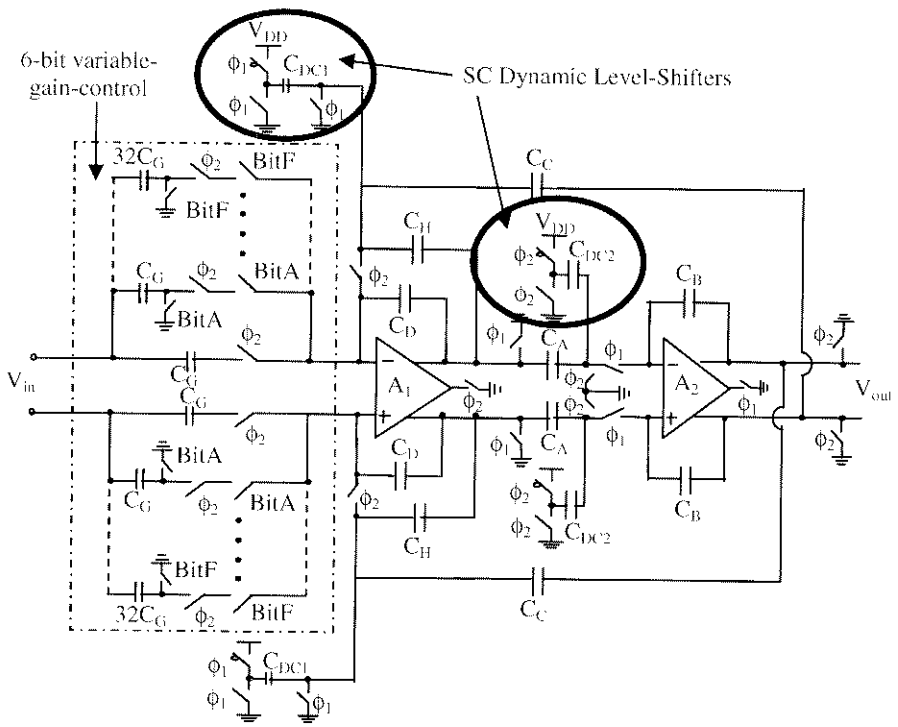


Figure 7.2 Proposed Switched-Opamp Biquadratic Filter with 6-bit Variable-Gain-Control

It can be observed that, due to the adoption of only half-delay SC integrators in the architecture, the two opamps A_1 and A_2 are only required to be active during their integration phases ϕ_2 and ϕ_1 respectively. As a result, these opamps can either be turned off or time-shared with other circuits after their integration phases to save power. A 6-bit (Bit-A to Bit-F) variable-gain-control circuit (VGC) is implemented by capacitor-ratio scaling at the input stage of the filter. For bandpass applications, it is possible to employ only

AC-coupling capacitors [BAS 97a, CHE 02b] as the input stage of the filter to maximize the input signal swing. It is because the AC-coupling capacitors do not impose a signal swing limit. Equation 7.1 describes the transfer characteristics of the proposed switched-opamp channel-select filter.

$$\frac{V_{out}(z)}{V_{in}(z)} = \frac{-C_A C_G (1 - z^{-1}) z^{-1}}{(C_D + C_H) C_B - [(2C_B C_D + C_B C_H - C_A C_C)] z^{-1} + C_B C_D z^{-2}} \quad \text{(Eq. 7.1)}$$

The denominator coefficients can be set by means of capacitor ratios to achieve for different bandpass filtering responses. In order to achieve a bandwidth of 1 MHz and a center frequency of 0.65 MHz while running at a sampling frequency of 10 MHz, a set of capacitors values are calculated and summarized in Table 7.2.

Table 7.2 Summary of Capacitor Values for SC Channel-Select Filter

C_A	0.11 p
C_B	0. 44 p
C_C	0.22 p
C_D	0.35 p
C_G (for 0-dB gain)	0.48 p
C_H	0.3 p
Capacitance Spread = $C_B/C_A = 4$	

A low capacitance spread of 4 is achieved. For 1-V operation, dynamic level-shifters [BAS 97a] (C_{DC1} and C_{DC2}) are employed to set the input and output common-mode DC operating points at 0 V and 0.45 V respectively. A 0-V input DC common-mode point favours the employment of a PMOS differential-pair as the input stage of the opamp. The output common-mode DC operating point of opamp is set at 0.45 V for circuit realization consideration to maximize the linear output swing.

7.4 Design of 1-V Switched-Opamp Ladder Filter

A fifth-order switched-capacitor ladder filter is employed to provide further attenuation of more than 12 dB and 30 dB at 1.65 MHz and 2.65 MHz respectively to fulfill the interference rejection requirement of the Bluetooth receiver. The filter is designed to have a –3-dB frequency of 1.5 MHz at a sampling frequency of 10 MHz. For low-power and low-voltage operation, the proposed half-delay-SC-integrator-based SC ladder filter, which is described in Chapter 3 section 3.5, is employed. Figure 7.3 shows the simplified switched-opamp realization of the fifth-order ladder lowpass filter,

which is derived from LCR-prototype [GRE 86] to achieve low passband sensitivity to element variations.

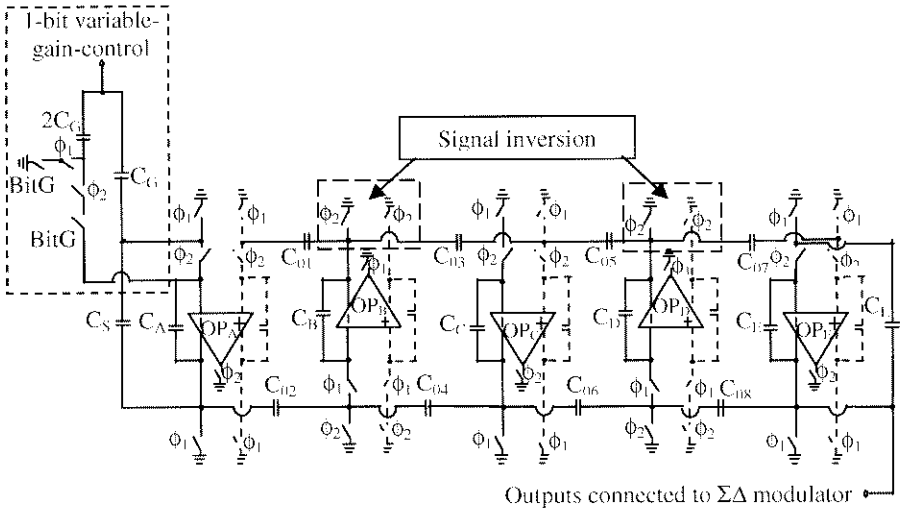


Figure 7.3 Proposed Switched-Opamp Ladder Filter with 1-Bit Variable-Gain-Control

As described in Chapter 3 Section 3.5, the key modification compared with conventional realization [GRE 86] is on the signal inversion at the outputs of the opamps OP_B and OP_D such that only half-delay SC integrators are used to implement the filter. By employing switched-opamp technique, all problematic switches are eliminated such that the filter can be implemented in a single 1-V supply. Besides, the opamps OP_A, OP_C and OP_E are required to be active during ϕ_2, while opamps OP_B and OP_D are only turned on during ϕ_1. This saves 50 % of the power consumption compared with a conventional SC ladder filter, which does not turn off the opamps after their integration phases. To avoid excessive loading effects to the switched-opamp channel-select filter, only 1-bit (Bit-G) variable-gain-control is employed at the input of the switched-opamp lowpass ladder filter. Table 7.3 summarizes the capacitor values of the proposed switched-opamp ladder filter.

Table 7.3 Summary of Capacitor Values for SC Channel-Select Filter

C_A	0.24 pF	C_{01}	0.2 pF
C_B	0.32 pF	C_{02}	0.2 pF
C_C	0.44 pF	C_{03}	0.2 pF
C_D	0.29 pF	C_{04}	0.2 pF
C_E	0.14 pF	C_{05}	0.2 pF
C_S	0.2 pF	C_{06}	0.2 pF
C_L	0.2 pF	C_{07}	0.2 pF
		C_{08}	0.2 pF

7.5 Design of 1-V Switched-Opamp Lowpass ΣΔ Modulator with Extended Noise-Shaping

For the Bluetooth receiver, the ΣΔ modulator must provide a signal-to-noise-ratio (SNR) of more than 9 dB for the analog-to-digital conversion for the interested frequency range of 0.15 MHz to 1.15 MHz (bandwidth of 1 MHz) while running at a low sampling frequency of 10 MHz to reduce power consumption. For this system, bandpass ΣΔ modulator [AZI 96, CHE 02b] cannot be employed since it requires the sampling frequency to be four times of the center frequency of the interested bandwidth. On the other hand, conventional lowpass ΣΔ modulators [COB 00, GER 00b] are only efficient for noise shaping at frequency range near the DC. In order to achieve for high resolution, either a large OSR (high sampling frequency) or a high-order ΣΔ modulator topology [AZI 96] must be employed. However, a high sampling frequency requires the circuits to run faster while a high-order topology needs more hardware, either ways dissipate much more power. In fact, for a conventional single-loop third-order lowpass ΣΔ modulator that operates at such a low over sampling ratio (OSR) of only 5, the signal-to-noise-ratio (SNR) is only 3 dB, which is insufficient. In order to employ a low sampling frequency of 10 MHz for the whole IF circuitry to reduce power consumption, as described previously in Chapter 3 section 3.6, noise-shaping extension technique can be applied to enhance the signal-to-noise-ratio (SNR) of the conventional ΣΔ modulator. Simulation result shows that, at a low OSR of only 5, the noise-shaping extension technique improves the SNR from 3 dB to 22 dB without acquiring extra active elements. Figure 7.4 shows the simplified schematic of the switched-opamp implementation of the proposed third-order ΣΔ modulator with noise-shaping extension for 1-V operation.

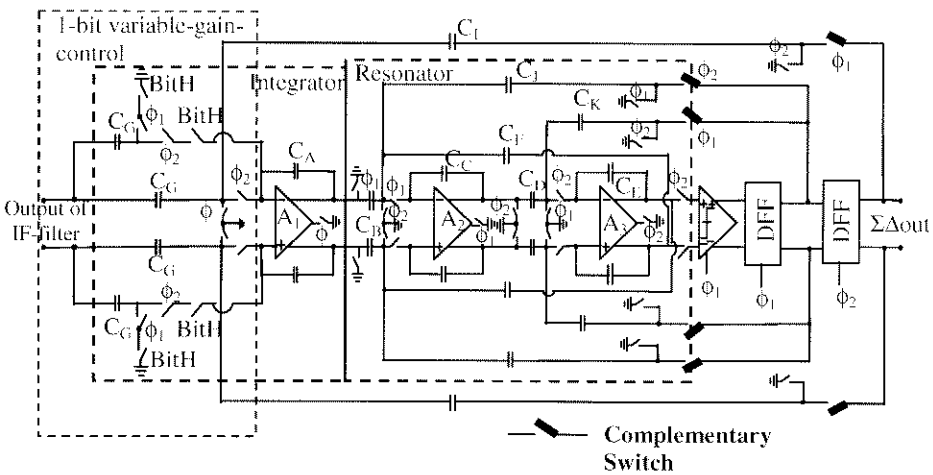


Figure 7.4 Half-Delay-Integrator-Based Lowpass ΣΔ Modulator with Noise-Shaping Extension

The ΣΔ modulator employs only half-delay SC integrators to reduce power consumption. It can be observed that the opamps OP_1, and OP_3 are required to be active during ϕ_2, while opamp OP_2 is only turned on during ϕ_1. This saves 50 % of the power consumption compared with conventional designs that employ full-delay integrator cells [COB 00, GER 00b, DES 01]. Extended noise shaping is achieved by employing an integrator to suppress the quantization noise at the DC and a resonator, which is placed at around 0.6 MHz, to notch out the quantization noise at low frequency. As a result, the noise-shaping region is extended and high SNR can be obtained even under a low OSR. A 1-bit (Bit-H) VGC is included at the input of the SO ΣΔ modulator to further enhance the linear range of the whole IF circuitry but not putting excessive loading effects to the switched-opamp lowpass ladder filter. Table 7.4 summarizes the capacitor values used.

Table 7.4 Summary of Capacitor Values for the Lowpass ΣΔ Modulator

C_A	0.5 pF
C_B	0.135 pF
C_C	0.5 pF
C_D	0.155 pF
C_E	0.5 pF
C_F	0.225 pF
C_G	0.25 pF
C_I	0.05 pF
C_J	0.09 pF
C_K	0.085 pF

7.6 Quadrature Channels Optimization

By employing switched-opamp techniques to implement the half-delay-SC-integrator-based filter and ΣΔ modulator, all the opamps employed in the IF circuitry can be turned off after their integration phases. As a result, the power consumption can be reduced as much as 50% compared with conventional SC implementation. Nevertheless, the input stage of the switchable opamp may be kept active at all time to achieve fast turn-on for high-speed operation as discussed in Chapter 4. Considering a typical two-stage opamp design, the input stage may burn 1/4 of the total power consumption of the opamp. Consequently, the power reduction is typically between 40 % to 50 % depends on the design of the switchable opamp.

To waive the extra power dissipation for maintaining the input stage of the switchable opamp always on, a deeper insight is put on the possibility to time-share the input stages of the opamps between the quadrature channels.

The sharing of the input stages of the opamps would also bring for better matching and faster operation. Considering two half-delay SC integrators that are employed respectively in the I-channel and Q-channel of the quadrature path as shown in Fig. 7.5.

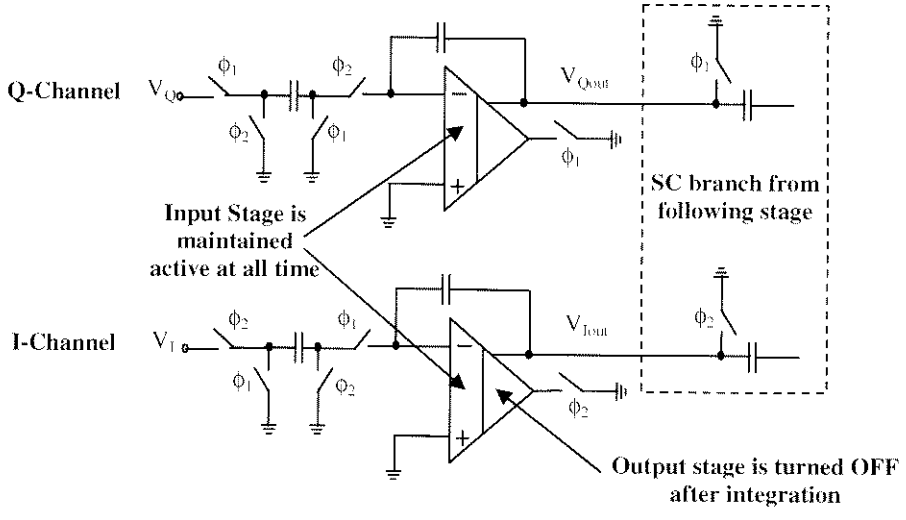


Figure 7.5 Two Half-Delay SC Integrators Operate in Alternate Clock Phases

By operating the quadrature channels in alternate clock phases, the half-delay SC integrators are therefore set to be operational alternately. In this sense, it is possible to time-share the input stages between the switchable opamps employed among the quadrature channels to save power and gain in better matching.

However, time-sharing of opamps could create a serious problem. This is due to the finite opamp gain, which left behind the residual errors at the opamp input terminals after each integration, therefore inevitably introduces coupling between the two channels and degrades the overall image rejection of the receiver. With this consideration, though it is possible to, the input stages of the opamps among the quadrature channels are not shared. Nevertheless, the output stages of the switchable opamps between the channels could still share a single current source for fast turn-on. This motivates the design of a dual-input switchable opamp to coherently avoid coupling of signals and allow time-sharing of the opamps between the quadrature channels, as discussed in next section.

7.7 Circuits Implementation

Figure 7.6 shows the proposed dual-input switchable opamp, which consists of dual two-stage operational amplifiers.

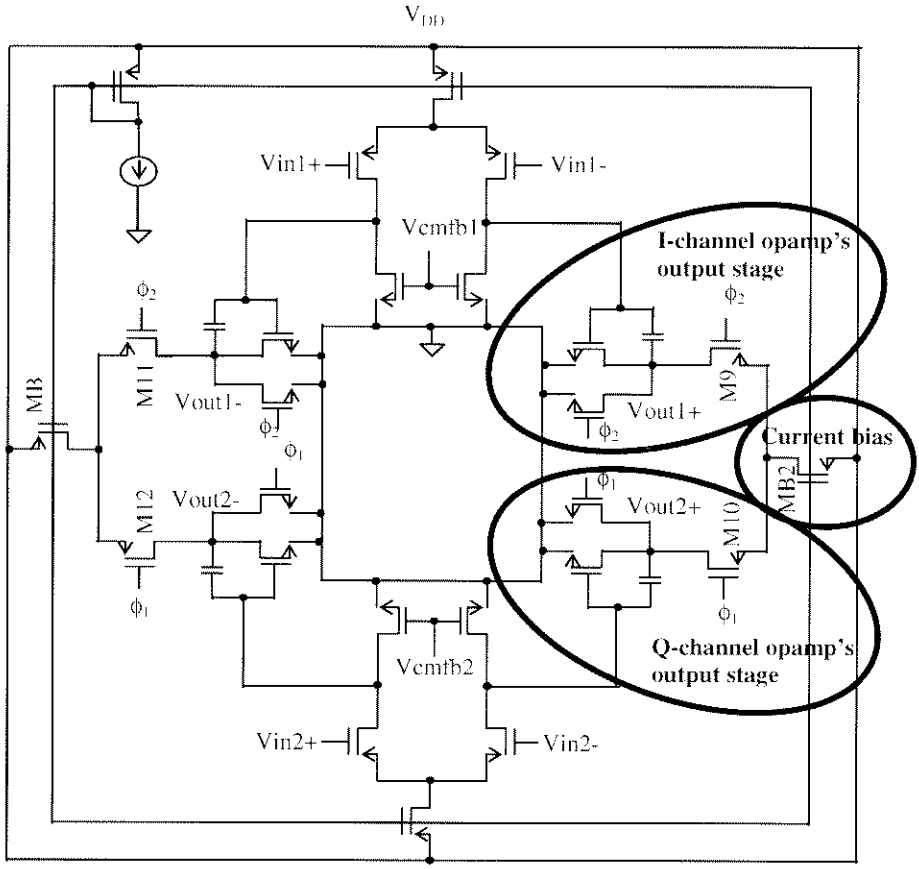


Figure 7.6 Proposed Dual-Input Switchable Opamp

The input stages of the opamps are made of PMOS differential-pairs with the common-mode input voltage set at ground. The output stages are controlled to turn on and off alternately using the differential switches M_9 and M_{11} (M_{10} and M_{12}) with a pair of complementary clock phases. The combination of the output stages at current sources M_{B1} and M_{B2} can significantly reduce the turn-on time of the output stages of the opamps. This is not only because the current sources M_{B1} and M_{B2} of the output stages are always kept active but also because the differential switches provide low output impedance at the turn-on instance and thus reduce dramatically the RC time constant associated at the opamp output node [CHE 02b]. For fast turn-off, additional NMOS switches are added at the outputs to pull them down to ground. Two

error-amplifier-based common-mode feedback circuits [PEL 97a] are employed to control the common-mode outputs voltages of opamp to 0.45 V for maximal linear output swing. Table 7.5 summarizes the measured performance of the switchable opamp.

Table 7.5 Summary of Measured Performance of the Proposed Switchable Opamp

Technology	0.35-μm CMOS
Supply Voltage	1 V
Low-Frequency Gain	65 dB
Unity-Gain Frequency	80 MHz
Phase Margin	47°
Max. Switching Frequency	15 MHz
Power Consumption	0.3 mW
Linear Output Swing	0.4 V
Loading Capacitor	1 pF

The measured low-frequency gain of the opamp is 65 dB, which is high enough to preserve the characteristics of the filters and ΣΔ modulator. The opamp is designed to have a maximum switching frequency of only 15 MHz, which minimizes the power consumption of the opamp while providing about 5-MHz margin. The design of the common-mode feedback circuit, comparator and D-flip-flop are similar as that presented in Chapter 6 section 6.6 and therefore are not repeated here.

7.8 Experimental Results

Figure 7.7 shows the chip photograph of the quadrature IF circuitry for the Bluetooth receiver.

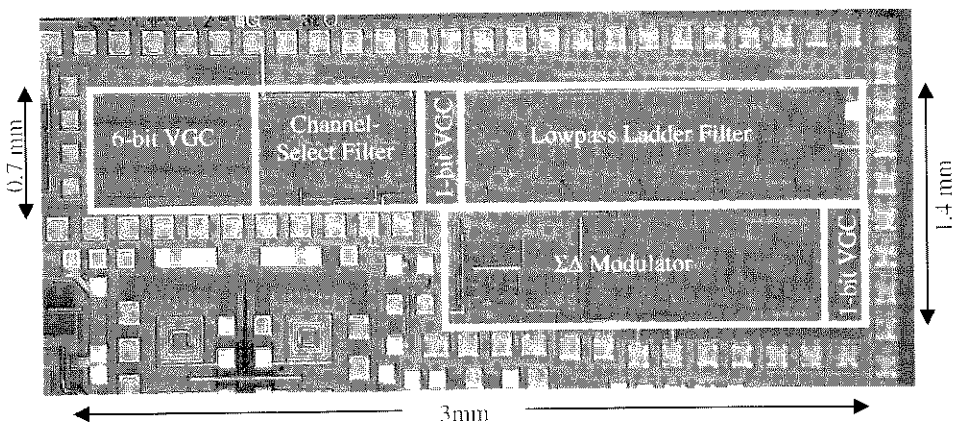


Figure 7.7 Chip Photograph of the IF Circuitry

The quadrature IF circuitry is implemented in a 0.35-µm CMOS double-poly four-metal process (V_{TP} = -0.77 V, V_{TN} = 0.6 V) and occupies a chip area of about 3.15 mm^2.

Figure 7.8 shows the measured frequency response of the whole IF-filter. The variable-gain-control for the whole IF filter is set at a nominal gain of 24 dB for the measurements. A 1-MHz bandwidth is obtained with –3dB corners located at 150 kHz and 1.15 MHz. The IF-filter provides an attenuation, with respect to the 24-dB passband gain, to interferences at 1.65 MHz and 2.65 MHz of more than 18 dB and 40 dB respectively, which well exceeds the Bluetooth specifications.

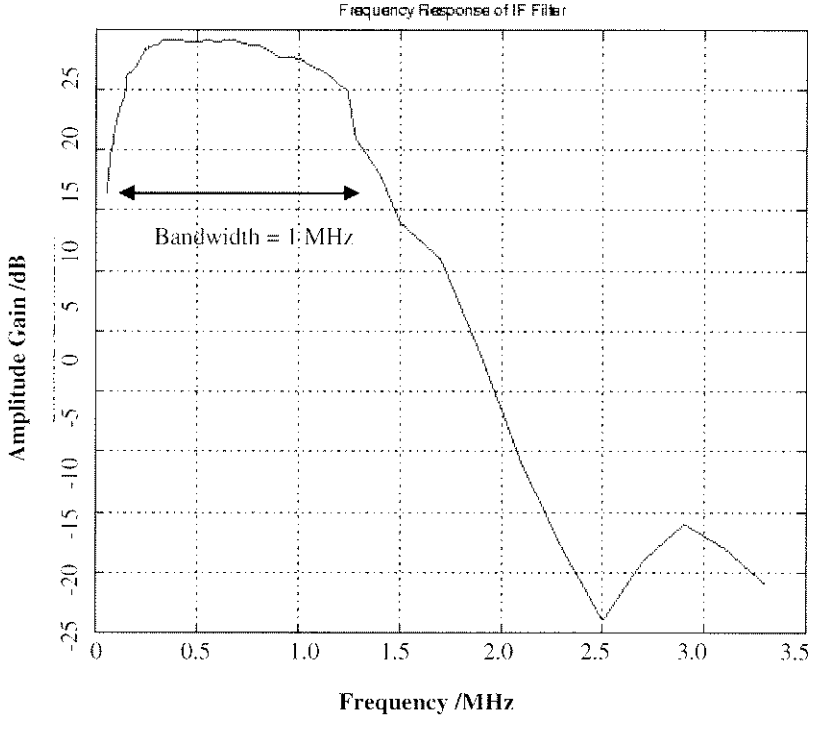


Figure 7.8 Measured Frequency Response of the IF Filter

The differential output transient response of the IF filter with a 240-kHz 0.5-V_{pp} in-band input with VGC sets at 0-dB gain is shown respectively in Fig. 7.9.

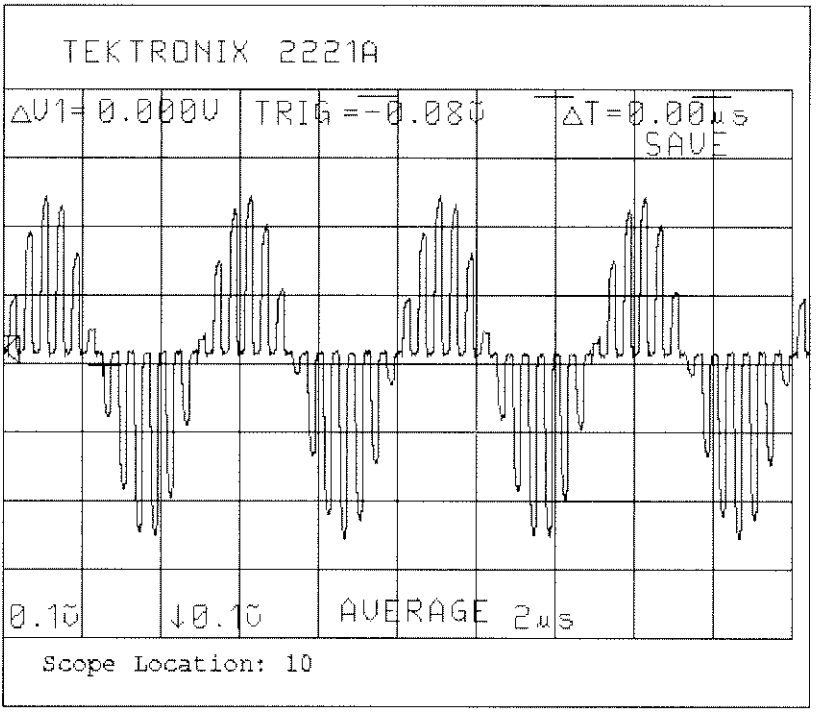


Figure 7.9 Differential Output Transient Response of IF Filter

Since the IF-filter is implemented with the switched-opamp technique. Therefore, a return-to-zero effect [BAS 97a, CHE 99] can be observed due to the shorting of the output of the opamps to the ground after the integration phase. The return-to-zero effect reduces the passband gain of the filter by 6 dB [CHE 00b] if the signal is processed continuously. Hence, it must be taken into account when the filter passband gain is designed.

A 42-dB variable gain control is measured for the IF filter with 6-dB step size. At a nominal gain of 24 dB, the IF filter achieves a 46-dB dynamic range at a 1-% third-harmonic distortion while dissipating 2.5 mW at a 1-V supply.

Figure 7.10 (a) and (b) show the full-span and in-band frequency spectrum of the ΣΔ modulator.

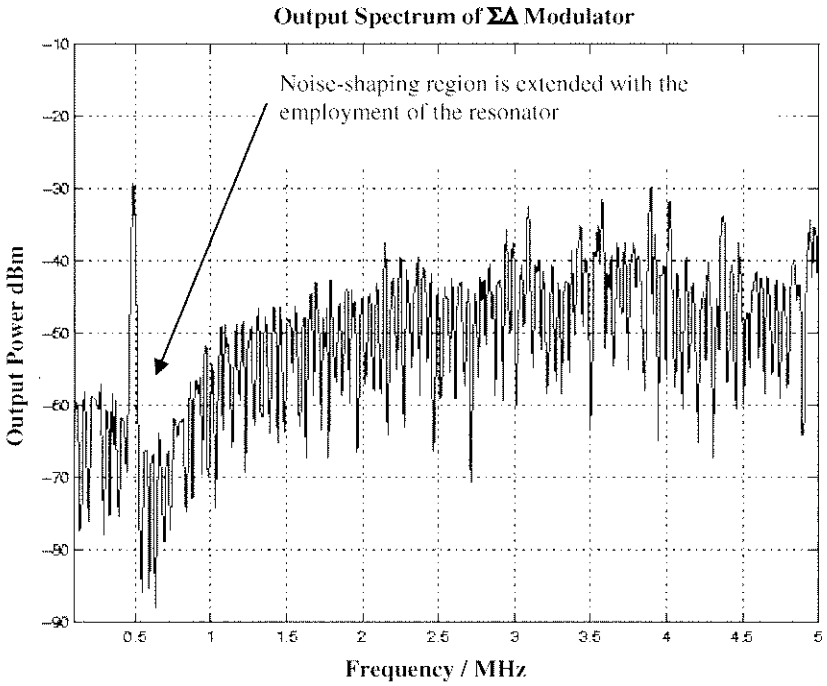


Figure 7.10 (a) Full-Span Output Spectrum of the ΣΔ Modulator

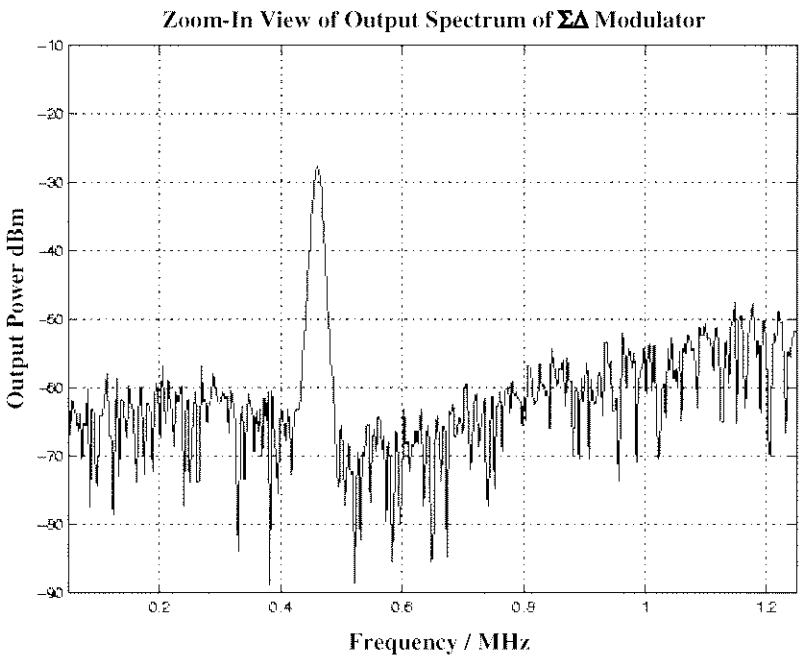


Figure 7.10 (b) In-Band Output Spectrum of the ΣΔ Modulator

The proposed ΣΔ modulator achieves a 3rd-order lowpass noise-shaping function. The interested signal bandwidth is 1-MHz (0.15 MHz to 1.15 MHz). It can be observed that with the placement of the resonator at 600 kHz position, the noise-shaping region is extended with quantization noise not more than –60 dB before 1.15 MHz. The extension of quantization noise suppression makes it possible to use a low oversampling ration (OSR) to achieve a high resolution, which can only be achieved with an increasing sampling frequency (OSR) with conventional topology.

Figure 7.11 plots the signal-to-noise-and-distortion (SNDR) ratio against the input signal level. A peak SNDR of 18 dB is achieved in a 1-MHz bandwidth and a sampling frequency of only 10 MHz. It shows a 20-dB improvement in the peak SNR compared with conventional third-order lowpass ΣΔ modulator topology without applying noise-shaping extension technique.

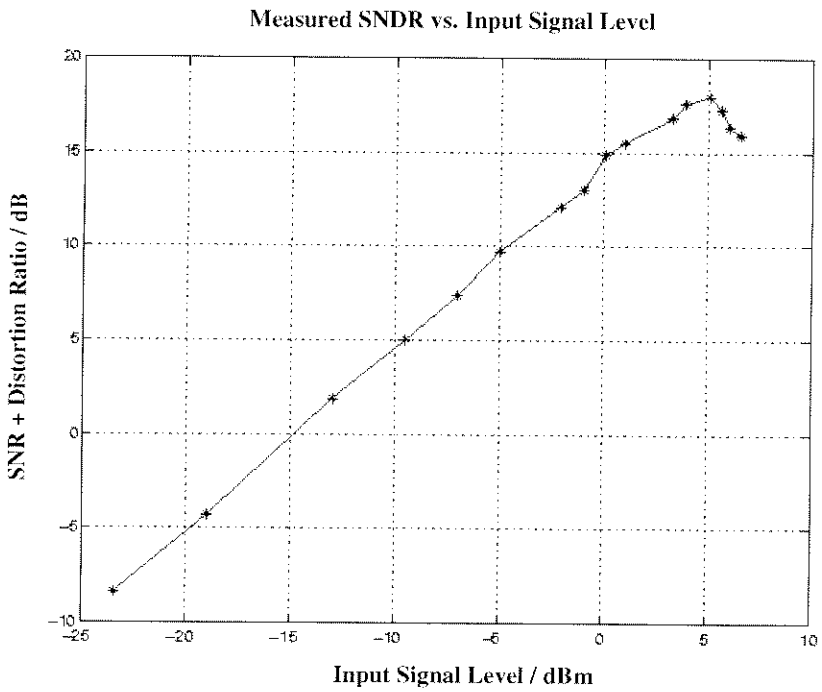


Figure 7.11 Measured SNDR vs. Input Signal Level

Figure 7.12 shows the 3% third-harmonic distortion (THD) for the IF circuitry. The 3% THD is obtained with a 240-kHz and 0.8-Vpp input signal with the VGC sets at 0-dB gain. The third-harmonic component is located at 720 kHz with an amplitude 30 dB lower the fundamental.

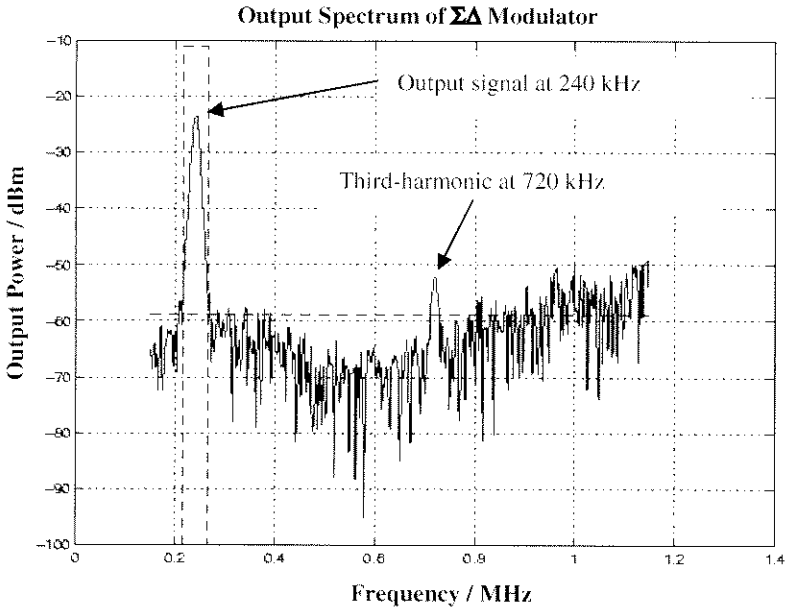


Figure 7.12 Output Spectrum at the ΣΔ Modulator Output Showing 3% THD

Figure 7.13 plots the IIP3 measurement result of the whole IF circuitry with the variable-gain-control circuit sets at a gain of 24 dB. In a 1-V supply, the whole IF circuitry achieves an IIP3 of better than -3 dBm for two tones at 1.65 MHz and 2.65 MHz with a power consumption of 3.5 mW.

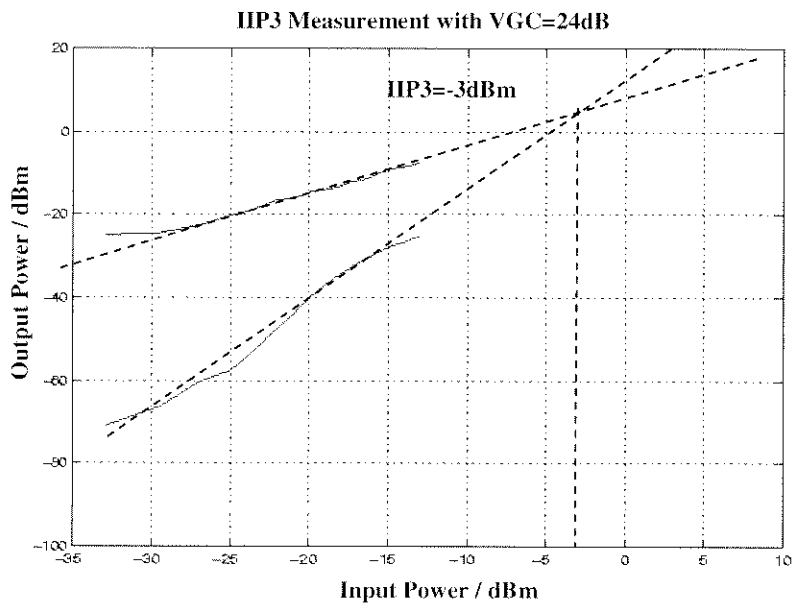


Figure 7.13 IIP3 Measurement of the Proposed IF circuitry at a Nominal Gain of 24 dB

Measurement result shows that the matching between the quadrature channels is better than 34 dB (2%), which is sufficient to fulfil the image rejection requirements. The circuits have also been successfully tested at a supply voltage of 0.9 V with proper operation. Figure 7.14 shows the output spectrum of the whole IF circuitry (measured at the output of the ΣΔ modulator).

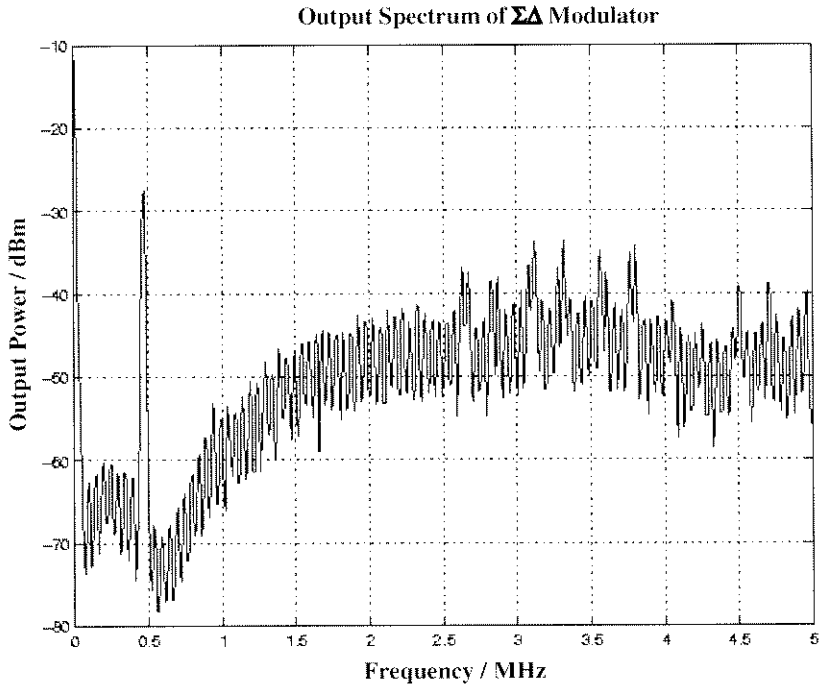


Figure 7.14 Output Spectrum of ΣΔ Modulator at a 0.9-V Supply

Though similar IF-filter frequency response is obtained, distortion increases a lot such that the IIP3 only reaches about –8 dBm at 0.9V operation. Also, the peak SNDR measured from the ΣΔ modulator reduces to 15 dB, which is marginally enough for Bluetooth receiver applications. Nevertheless, the 48-dB variable-gain-control still works properly and the power consumption reduces to 2.6 mW. Table 7.6 summarizes the performances of the proposed quadrature IF circuitry.

Table 7.6 Performance Summary of the Proposed Quadrature IF Circuitry

Technology	0.35-μm double-poly 4-metal CMOS process
Supply Voltage	1 V
Filter Bandwidth	1MHz
Channel Matching	34 dB (2%)
Variable-Gain-Control	0dB to 48dB 6dB per step
Linearity	- 3dBm @ 24 dB Gain
Dynamic Range @ Filter	48dB @ 3% IM
Peak SNR	18 dB
Power Consumption	3.5 mW
Chip Area	3.15 mm^2

7.9 Conclusion

A single 1-V switched-opamp IF circuitry for Bluetooth receiver is implemented based on half-delay SC integrators to improve channel matching and reduce power consumption. To further reduce the power consumption of ΣΔ modulator, a novel noise-shaping extension technique is proposed to achieve high resolution with low OSR. At a 1-V supply, the IF circuitry consumes only 3.5 mW, which makes it very attractive for most portable applications. With the availability of low-voltage CMOS front-end circuits, single 1-V CMOS wireless transceivers maybe available in recent future.

Chapter 8

DESIGN OF ULTRA-LOW-POWER SINGLE-SWITCHED-OPAMP-BASED SYSTEMS

8.1 Introduction

In the past decade, biomedical ICs have been playing an important role in medical treatment such as pacemaker applications [SAN 96]. The biomedical ICs must be:

Compact to be implanted into body
Ultra-low-power to extend battery life
Tiny-size and highly reliable.

CMOS technologies are always good candidates for low-cost, low-power and reliable IC designs. The feasibility of integrating both analog and digital circuits in single-chip makes CMOS technologies possible for compact designs in low cost. In recent years, a few numbers of low-power biomedical ICs have been employing switched-capacitor (SC) circuits for signal selection and digitization [CAS 90b, GER 00a, BAS 00]. In fact, SC circuits guarantee high performance accuracy and provide high dynamic range due to the use of highly-matched-and-linear integrated capacitors. Besides, switched-opamp techniques [CRO 94, BAS 97a, CHE 99] show robust and good performance for operating SC systems at low supply voltages, which allow biomedical ICs to operate at sub-1-V region. The lowering of supply voltages can reduce the power consumption as well as the size of battery, thus improving the chip's implantability. Lastly, biomedical applications usually require SC circuits to work only in a few kHz sampling frequency, which makes it possible to operate in a few μW.

In fact, at a sampling rate of a few kHz, the power consumption of a SC circuit is primarily determined by the number of opamps count. On the other hand, the current draw of an opamp is mainly lower limited by, system-wise,

the speed and noise requirements; and technology-wise ...age current of the devices. For micro-power operation, the opamp ...ed to cope with the leakage current and noise requirement while th... are actually over-designed in term of speed. As a result, convent... rchitectures that employ multiple opamps would have power dis... a few-μW ranges [BAS 00, GER 00a].

Intuitively, time-multiplexing one over-designed opa... ze a high-order SC system would give the best compromise an..., noise and leakage current requirements while possibly reduci... tem power consumption. However, the amount of the time multi... opamps is usually limited by the conventional SC architecture th... num of two opamps is required to work alternately [CAS 90b]. On... hand, most of the previous reported opamp-time-multiplexed desig... 95] employ high supply voltages and suffer from the stability problem... e to open-loop connection of the opamp during the period between non-overlapping clock phases where the change of the integrator capacitors occurs as a result of time multiplexing. Conventionally, the problem could be solved by employing XY feedback technique [ANA 95], which, however, adding additional capacitive loads at both input and output of an opamp. Thus making the opamp run slower. In this chapter, two single-opamp-based designs for pacemaker applications are presented. The focus is put on further power reduction to the sub-μW range while achieving robust operation at low supply voltages.

8.2 System Considerations

Figure 8.1 shows the block diagram of the proposed SC signal-conditioning system for pacemaker applications.

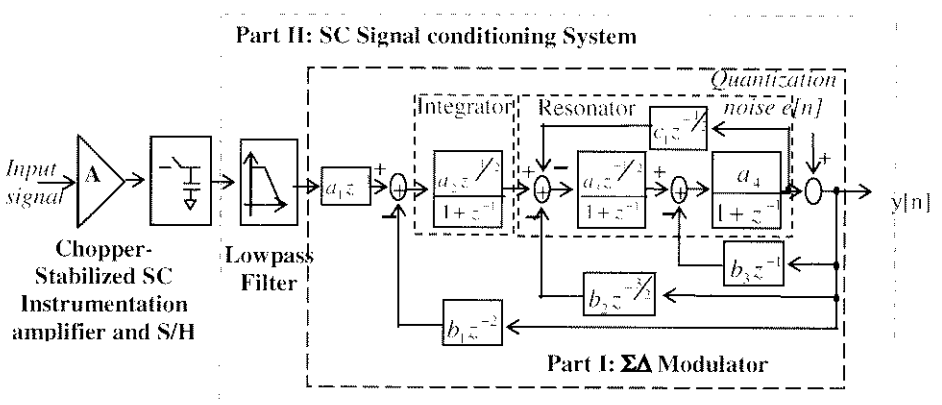


Figure 8.1 Proposed SC Signal Conditioning System

A double-correlated-sampling [KAJ 01, WAN 01] SC chopper-stabilized sample-and-hold circuit works as an instrumentation amplifier to preamplifier the signal to a detectable level. The SC lowpass filter achieves a cut-off frequency of about 100 Hz to suppress the interference [BAS 00]. The selected signal is digitized in high resolution with a ΣΔ modulator. In order to reject the noisy common-mode signals like power supply noise and clock feed-through noise, fully-differential architecture is adopted.

In the first part of this chapter, the design of a single-opamp-based 3rd-order lowpass ΣΔ modulator is described. Sub-μW operation at a single 0.9-V supply is achieved by employing the multi-phase switched-opamp (SO) technique [CHE 00b], which, as will be discussed further on, intrinsically guarantees stable operation for single-opamp designs in a 0.9-V supply without employing XY feedback technique. In the second part of this chapter, the possibility of integrating a complex SC system by time-multiplexing one opamp will be demonstrated through the design of a SC signal conditioning system, which consists of a 3rd-order ladder lowpass filter cascaded with a 3rd-order lowpass ΣΔ modulator with extended noise-shaping.

8.3 Design of a 0.9-V Sub-μW SC ΣΔ Modulator

In this section, a sub-μW ΣΔ modulator is demonstrated for pacemaker applications. The modulator employs a half-delay-SC-integrator-based 3rd-order single-loop topology, which was described in Chapter 3 section 3.7, to achieve high power efficiency. To further reduce the power consumption, a single-opamp (SOP) realization is proposed to reduce the opamp count. Figure 8.2 shows the proposed time-multiplexing scheme for the half-delay-SC-integrator-based switched-opamp ΣΔ modulator.

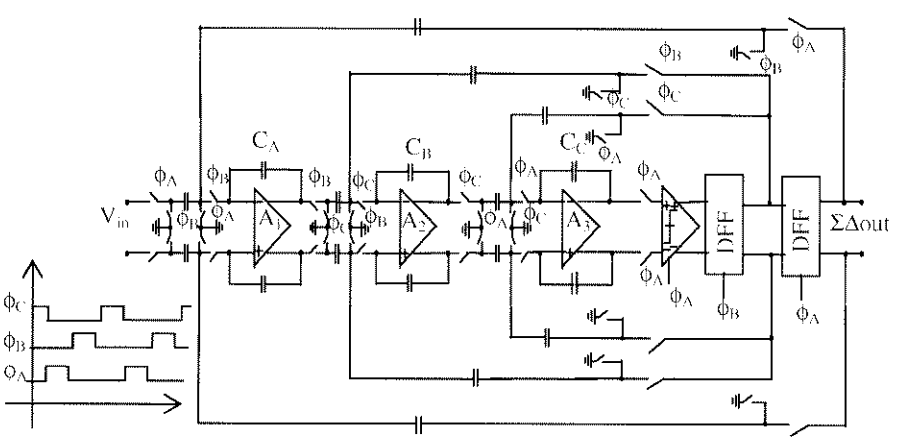


Figure 8.2 SC Implementation of the Half-Delay-Integrator-Based Lowpass ΣΔ Modulator

The opamps A_1, A_2 and A_3 are realizing half-delay integration function for the ΣΔ modulator at on-chip non-overlapping clock phases ϕ_B, ϕ_C and ϕ_A respectively. It can be observed that, due to the use of half-delay integrators, these opamps can be turned off after their integration phases to reduce power significantly. With this special clock phase arrangement, only one of the three opamps is required to be active at a time. As a result, with proper time-multiplexing scheme, single opamp can be employed to replace all these opamps.

8.3.1 Single-Opamp-Based ΣΔ Modulator Topology

Figure 8.3 shows the simplified single-switched-opamp-based (SSOP) design of the 3rd-order lowpass ΣΔ modulator.

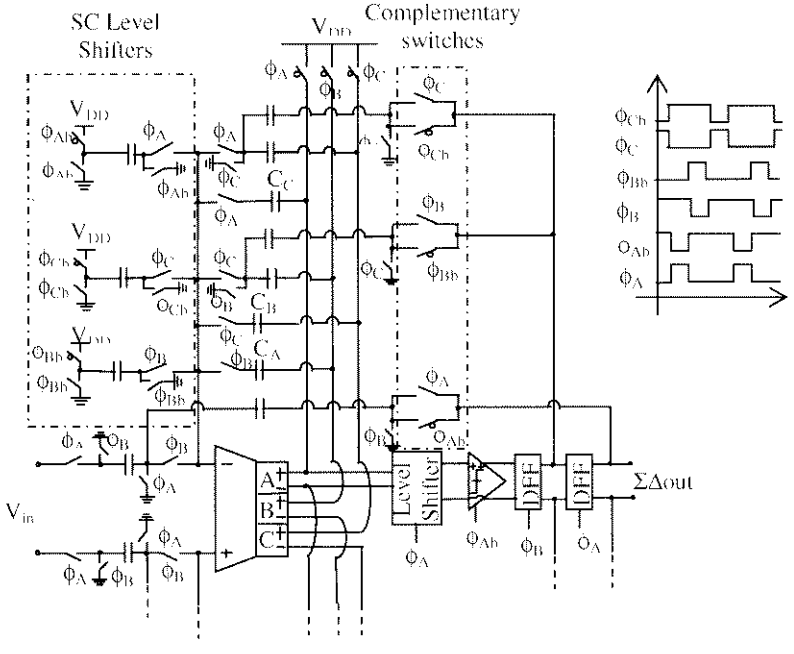


Figure 8.3 Schematic of the Proposed Single-Opamp-Based ΣΔ Modulator (Single-ended is shown)

To cope with the low supply voltage requirement and multi-phase operation, multi-phase switched-opamp technique is employed. The proposed SOP ΣΔ modulator employs an opamp with three switchable output stages, which are turned on and off alternately with three on-chip non-overlapping clock phases ϕ_A, ϕ_B and ϕ_C. (ϕ_{Ab}, ϕ_{Bb} and ϕ_{Cb} are the complementary clock phases of ϕ_A, ϕ_B and ϕ_C respectively). The integrator capacitors C_A, C_B and C_C are connected in feedback with the opamp during their integration phases, but

kept open-connected to preserve their stored charge for next integration event. Dynamic SC level-shifters are employed to bias the common-mode voltages of the opamp input and output at ground and $V_{DD}/2$ respectively. The analog output of the opamp is passed at ϕ_A to a latch-type comparator with a SC level shifter. The comparator is reset at ϕ_{Ab} and its output is then stored by D-flip-flops (DFF). Since the outputs of the DFFs are either V_{DD} or ground, complementary switches can be employed to feed the DFFs output back to the opamp.

8.3.2 Switchable Opamp Design

To achieve high-efficient SSOP design, a novel two-stage operation amplifier with three-switching-output-pairs is proposed for the implementation. Figure 8.4 shows the schematic of the proposed switchable opamp.

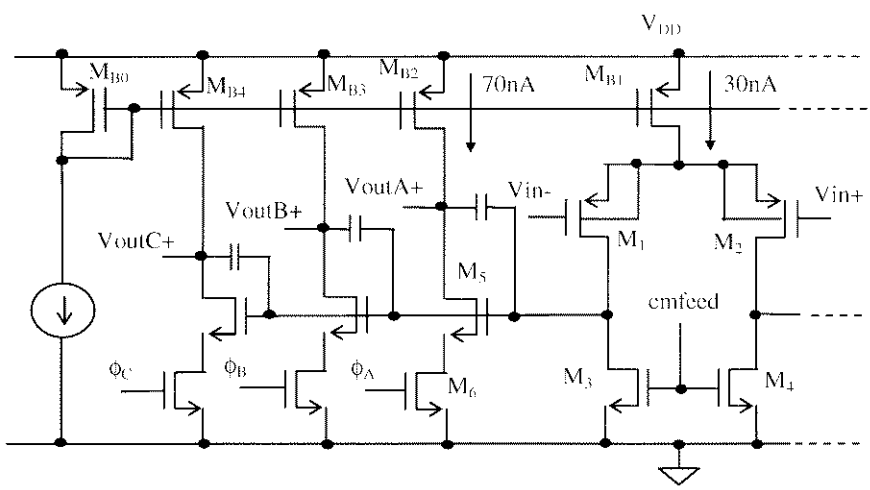


Figure 8.4 Proposed Opamp with Three Switchable Output Pairs (Single-ended is Shown)

To reduce the supply voltages and Flicker's noise effect, a PMOS differential pair operates at sub-threshold region is employed as the input stage. In an N-well process, it is possible to connect the bodies of the input transistors to their sources rather than connecting to the highest supply voltages to reduce the body effect, where the latter case increases the threshold voltages of the device. Implemented in a standard 0.35-μm CMOS process (VT_P = -0.77 V, VT_N = 0.6 V) and at a 0.9-V supply, the common-mode input voltage is set at ground. Three identical switchable output pairs are controlled to turn on and off alternately by three non-overlapping clock phases ϕ_A, ϕ_B and ϕ_C. Each of

the output stages is connected to a compensation capacitor to stabilize the opamp when the output stages are turned on. Since only one output pair is turned on at a time, the differential output stage dissipates only 140 nA. Take into account the 30 nA current dissipation from the input stage and 15 nA current draws from the biasing circuit, the opamp consumes only 185 nA. At a 0.9-V supply, the opamp achieves a measured DC gain of 75 dB and a unity-gain bandwidth of 50 kHz at 1-pF loading. Table 8.1 and Table 8.2 summarize the device size and the measured performance of the opamp respectively.

Table 8.1 Summary of Device Size

Transistors	Unit Size (W/L)	Quantity
M_{B0}	0.8μ/6μ	X2
M_{B1}	0.8μ/6μ	X4
M_{B2}	0.8μ/6μ	X8
M_1, M_2	0.8μ/6μ	X2
M_3, M_4	0.8μ/8μ	X2
M_5	0.8μ/8μ	X8
M_6	2μ/0.4μ	X8

Table 8.2 Measured Performance of the Opamp

Supply Voltage	0.9 V
Low Frequency Gain	75 dB
Unity Gain Bandwidth	50 kHz
Phase Margin	46°
Linear Output Swing	0.5 V
Power Consumption	200 nW
Core Chip Area	300μm x 200 μm
Loading	1 pF

8.3.3 Dynamic Common-Mode Feedback Circuit

Figure 8.5 shows the common-mode feedback circuit (CMFB) for the proposed opamp. SC level-shifters are used to compute the common-mode output voltage of the opamp and inject the result to the error-amplifier-based CMFB [WAL 99], which is built with a differential-pair. The error signals are fed back to the opamp input stage at V_{cmfeed} to control the opamp output common-mode voltage to $V_{DD}/2$. The current consumption of the CMFB is 15 nA.

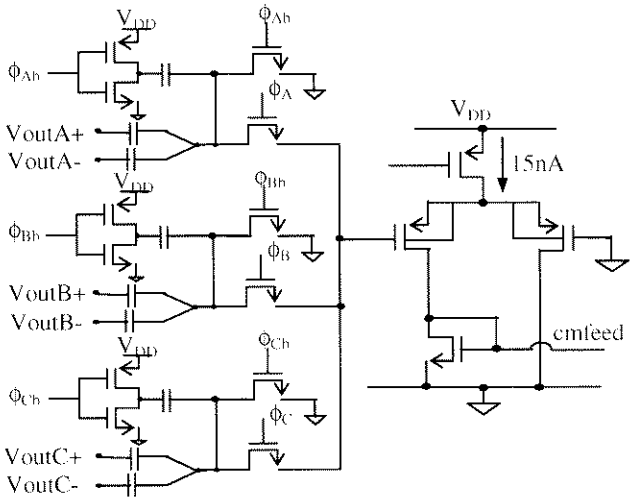


Figure 8.5 Proposed Dynamic CMFB Circuit

8.3.4 1-V Latch-Type Comparator

The schematic of the 1-V latch-type sub-threshold-region-operated comparator with NMOS regenerative pair is shown in Fig. 8.6.

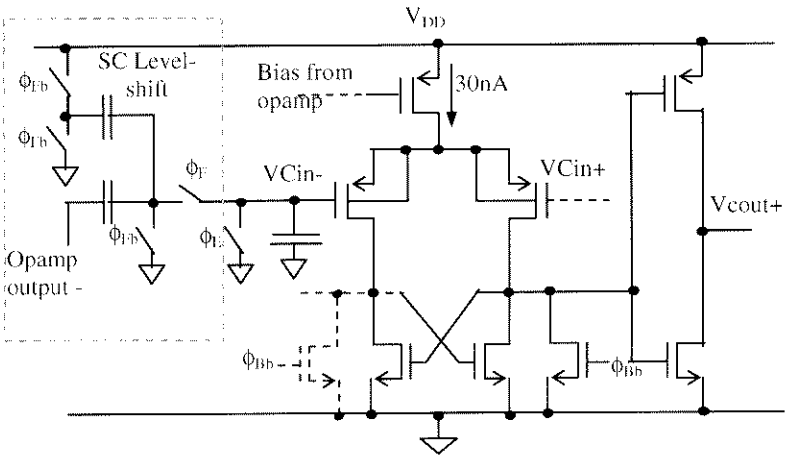


Figure 8.6 1-V Latch-Type Comparator Operates at Sub-Threshold Region (Single-end is shown)

SC level-shifters are used not only to suit the different DC-biasing of the opamp output nodes and the input nodes of the comparator, but also to provide appropriate reference level for the comparator. The comparator receives the output of the opamp at ϕ_{I}, which corresponds to the output of the last integrator of the ΣΔ modulator. Comparison is done during ϕ_{B}, which is the next clock phase after ϕ_{I}. The output of the comparator is then latched by a DFF at ϕ_{B}. The comparator is reset with two mechanisms in order to match with the time-multiplexing scheme of the system without employing additional clock phases. The NMOS regenerative pair is reset to ground during ϕ_{BB} is high. This guarantees the comparator will only make comparison at ϕ_{B}. On the other hand, the inputs of the comparator are also reset to ground during ϕ_{E} just after finished the comparison, where ϕ_{E} is the next clock phase after ϕ_{B}. The comparator shares the same current bias with the opamp and dissipates 30 nA.

8.3.5 Experimental Results of the SSOP ΣΔ Modulator

Figure 8.7 shows the chip photograph of the proposed SSOP ΣΔ modulator, which is implemented in a 0.35-μm CMOS double-poly four-metal process (VT_N = 0.6 V, VT_P = -0.77 V) and occupies a chip area of about 0.14 mm^2.

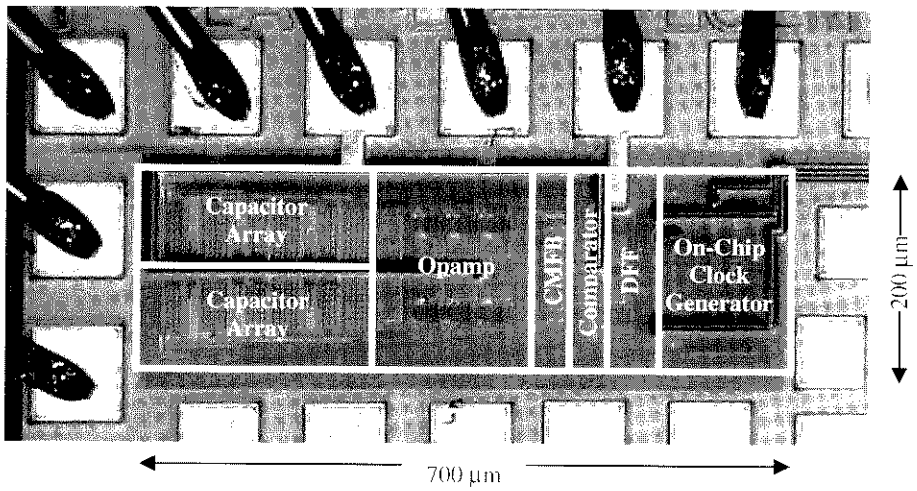


Figure 8.7 Chip Photograph of the Proposed DS Modulator

Poly-to-poly capacitors are used for good linearity. All capacitors are distributed evenly at two sides and laid out close together for good matching. The analog circuits (opamp and switched-capacitors) are placed at the left hand side surrounded by a guard ring to minimize the switching noise

coupling from the digital parts (comparator and DFFs), which are placed at the right hand side of the layout.

Figure 8.8(a) shows the testing setup for characterizing the ΣΔ modulator. A FFT network analyzer (SR770, Stanford Research Systems) is employed to generate the input signal and capture the output frequency spectrum of the ΣΔ modulator.

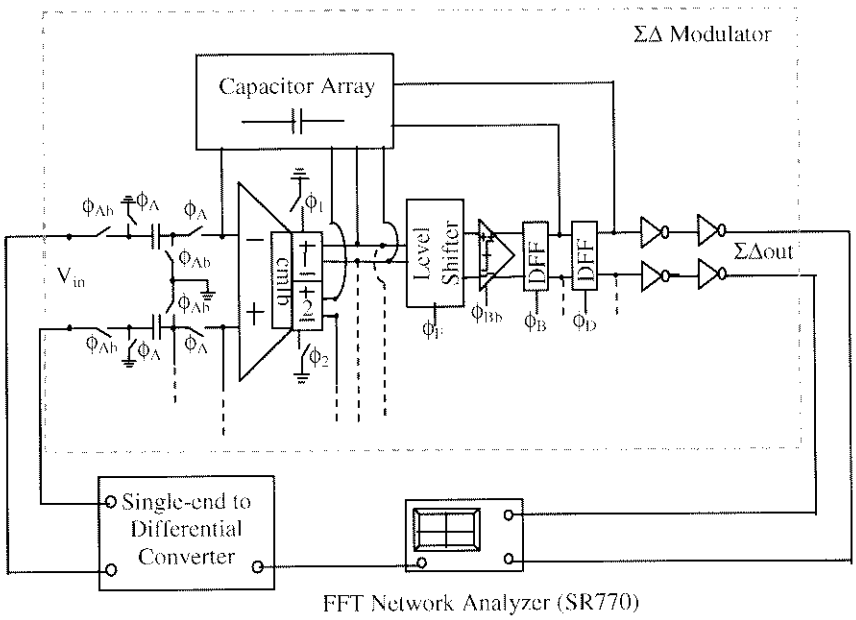


Figure 8.8 (a) Testing Setup for the Proposed DS Modulator

Figure 8.8(b) shows an off-chip single-end-to-differential converter to generate the required differential signal to the ΣΔ modulator. Two opamps (Op. 07, MAXIM Inc.) are configured identically, but one operates in non-inverting mode while the other one operates in an inverting mode by applying the source signal at different nodes. Variable resistors are employed to obtain the best matching of the generated differential signals. Further processing of the stored frequency spectrum is then carried out with Matlab to obtain the corresponding signal-to-noise-ratio (SNR).

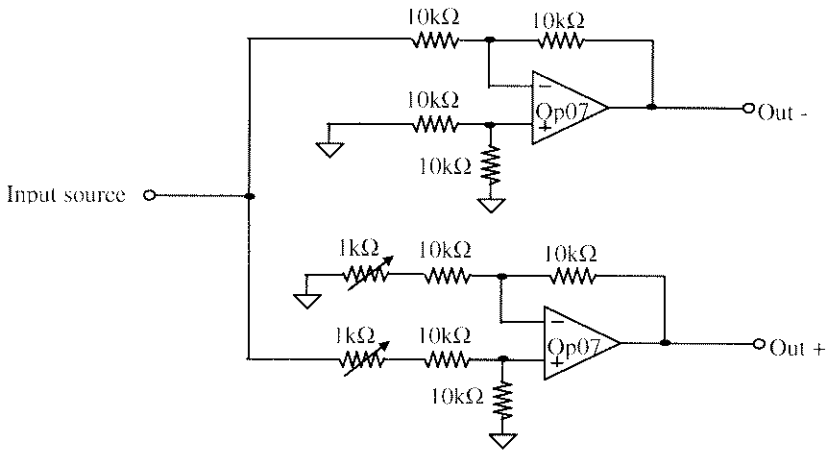


Figure 8.8 (b) Single-End to Differential Converter

Figure 8.9 plots the full-span view of the measured output frequency spectrum of the ΣΔ modulator operated at 0.9-V supply with an input frequency of f_{in} = 26.12 Hz. A system clock frequency of 30 kHz is applied to the on-chip clock generator to operate the ΣΔ modulator at an effective sampling frequency of 10 kHz under the proposed time-multiplexing scheme. A 3rd-order lowpass noise-shaping function is obtained as designed, which verifies that the possibility to time-share one opamp to realize high-order ΣΔ modulator.

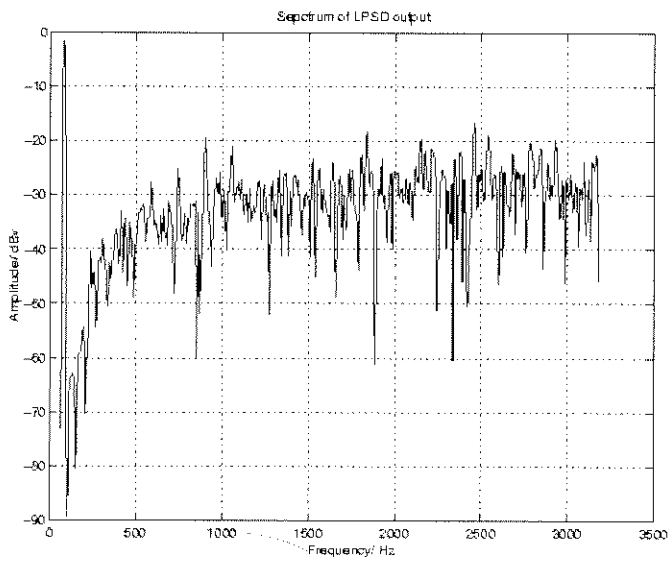


Figure 8.9 Measured Output Spectrum (Full-Span View) of the Proposed Single-Switched-Opamp-Based ΣΔ Modulator

Figure 8.10 plots the zoom-in view of the frequency spectrum of the ΣΔ modulator with a –14-dBV 26.12-Hz input signal at which the peak SNDR is obtained. The third-harmonic component of the input signal is located at $3*f_{in}$ = 78.36 Hz, which is inside the interested 70-Hz bandwidth centred at 55 Hz, and is measured to be 71 dB below the fundamental. The ΣΔ modulator is designed to operate at a sampling frequency of 10 kHz such that the noise floor is dominated by the thermal noise of the opamp but not the quantization noise. This would maximize the achievable SNR at a given power consumption.

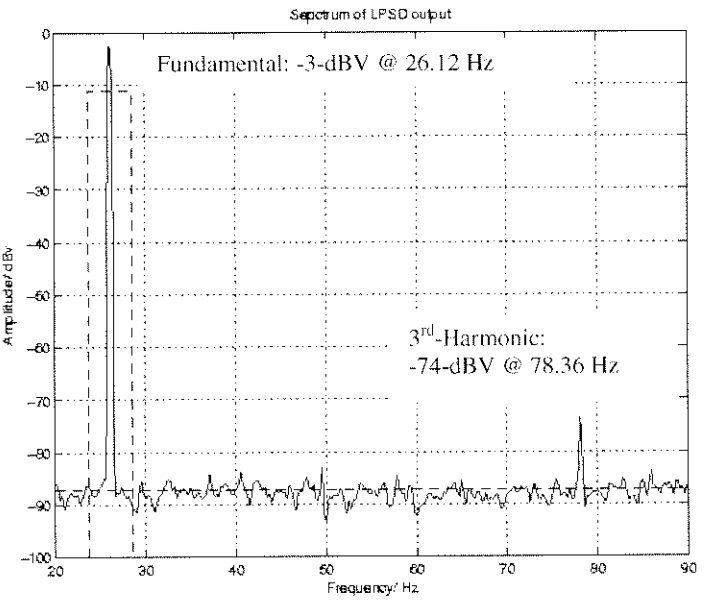


Figure 8.10 Measured Output Spectrum (Full-Span View) of the Proposed Single-Switched-Opamp-Based ΣΔ Modulator

Figure 8.11 plots both of the signal-to-noise-ratio (SNR) and the signal-to-noise-plus-distortion-ratio (SNDR) of the ΣΔ modulator as a function of ratio of the input level over the reference voltage (Vref). A reference voltage of $V_{DD}/2$ is employed for the ΣΔ modulator. At 0.9-V operation, the measured SNR is 60.2 dB at an input level of –13 dBV. The corresponding dynamic range of the ΣΔ modulator is 64 dB, which is equivalent as 10.7-bit resolution. The measured peak SNDR is 60 dB with a bandwidth of 70 Hz (20 Hz to 90 Hz) at an input level of –14 dBV. The SNDR is limited by the significant increase in harmonic distortion at input magnitude larger than –14 dBV. The distortion is caused by the limited output swing of opamp of only 0.5 V. The total power consumption is only 0.4 μW where the opamp dissipates 0.2 μW while the digital circuitry (including clock generator) dissipates 0.2 μW using a master clock frequency of 30 kHz.

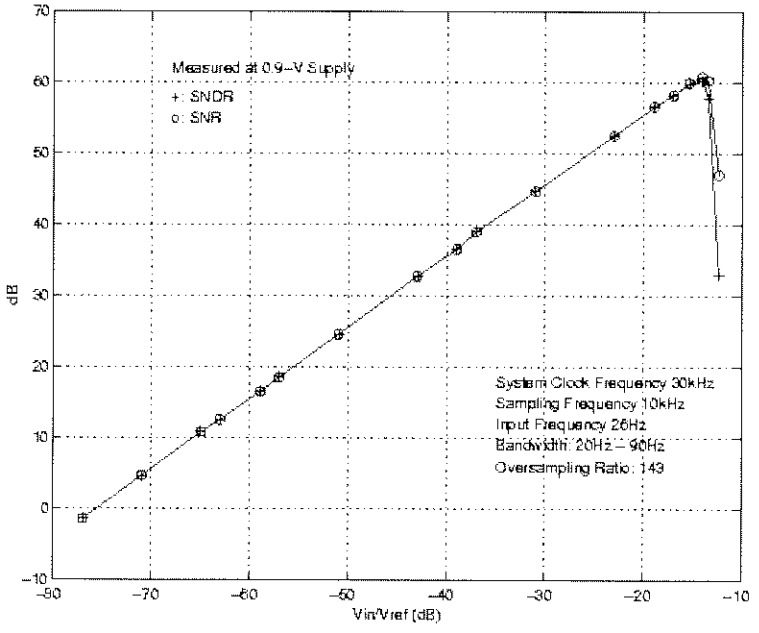


Figure 8.11 Measured SNR and SNDR vs. Input Signal Level at 0.9-V Operation

Theoretically, with a bandwidth of 70 Hz and a sampling frequency of 30 kHz, the over-sampling-ratio (OSR) is about 143, and the maximum achievable SNR of this 3rd-order lowpass ΣΔ modulator is about 83 dB. Hspice simulation result shows an achievable peak SNDR of 75 dB with an input magnitude of −14 dBV. The difference between calculation and simulation could be caused by several factors, namely the non-linear behaviours of the ΣΔ modulator and the non-idealities of the circuit performance such as distortion. The measurement result is 15 dB lower than the simulation result mainly because the simulation did not take into account the thermal noise from the opamp.

To show the robustness of the ΣΔ modulator, measurement results at supply voltages of 0.8 V, 1.0 V and 1.2 V are obtained. Figure 8.12 (a), (b) and (c) plots the measured SNR and SNDR of the ΣΔ modulator as a function of ratio of the input level over the reference voltage (Vref) at a supply voltage of 0.8 V, 1.0 V and 1.2 V respectively. The measured SNR and SNDR of the ΣΔ modulator at 0.8-V operation are both 55 dB, which are about 5 dB lower than the measurement results at 0.9-V operation. This is primarily due to the reduction of the supply voltage from 0.9 V to 0.8 V, which reduces the available output swing of the opamp. As a result, there is more distortion even at lower input level, which in turns reducing the resolution of the ΣΔ modulator.

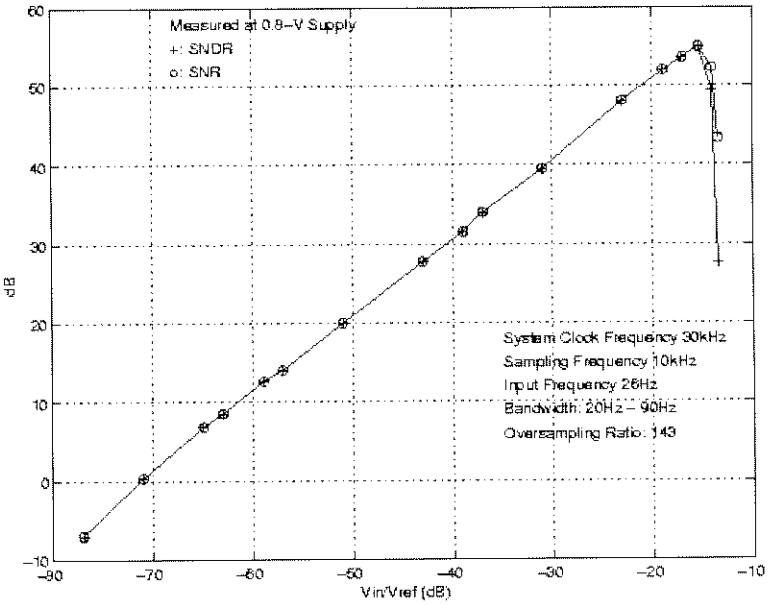


Figure 8.12 (a) Measured SNR and SNDR vs. Input Signal Level at 0.8-V Operation

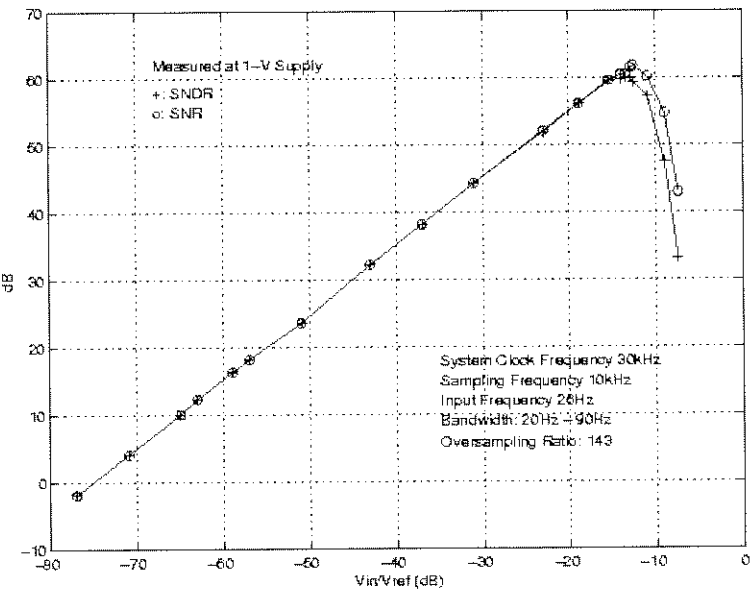


Figure 8.12 (b) Measured SNR and SNDR vs. Input Signal Level at 1.0-V Operation

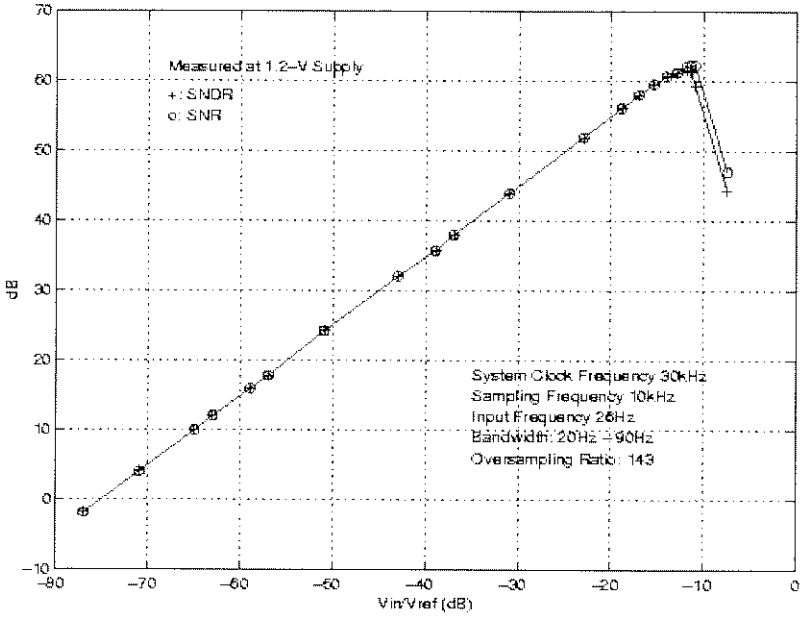


Figure 8.12 (c) Measured SNR and SNDR vs. Input Signal Level at 1.2-V Operation

On the other hand, when supply voltage is increased from 0.9 V to 1.0 V, the SNR of the ΣΔ modulator is improved by about 2 dB due to the increase of the output swing of the opamp at higher supply voltages. Besides, a 3-dB resolution enhancement is also obtained when a supply voltage of 1.2 V is employed. Table 8.3 summarizes the performance of the ΣΔ modulator.

Table 8.3 Summary of Measured Performance of the ΣΔ Modulator [CHE 02a]

Technology	0.35-μm CMOS			
Supply Voltage	0.8 V	0.9 V	1.0 V	1.2 V
Topology	Single-Loop 3rd-Order Lowpass			
Sampling Frequency	10 kHz			
Bandwidth	20 to 90 Hz			
SNR	55 dB	60.5 dB	61.8 dB	62.3 dB
SNDR	55 dB	60.2 dB	60.4dB	61.53 dB
Dynamic Range	57 dB	62.5 dB	66 dB	67 dB
Power Consumption	180 nW	200 nW	220 nW	240 nW
Core Chip Area	200μm x 700μm			

8.4 Design of a 0.9-V Sub-μW SC Signal Conditioning System

In this section, a 0.9-V single-opamp-based SC signal conditioning system [CHE 03a] for pacemaker applications is presented. The proposed SC signal-conditioning system consists of a 3rd-order ladder lowpass filter cascaded with a 3rd-order lowpass ΣΔ modulator as described previously in Fig. 8.1. The lowpass SC ladder filter is synthesized from a 3rd-order LCR prototype filter to achieve a Chebyshev 3rd-order lowpass response with a passband ripple less than 0.5 dB to preserve the phase and amplitude information of the signals. The filter is cascaded with a noise-shaping-region-extended 3rd-order lowpass ΣΔ modulator, which consists of an integrator and a resonator. In a conventional implementation, six opamps are usually required to implement this sixth-order SC system [GRE 86, KI 95]. Besides, these six opamps would be required to be active at all time. Due to the noise and leakage current limitations, each opamp would have to consume a minimum current (I_B). It is likely that, at this current consumption, the opamp is over-designed in terms of speed requirement. As a result, the system burns a fundamental current consumption of $6I_B$, for which the opamps maybe running at a speed that is higher than required. For such an integrated system, the possibility and potential improvement of scaling the requirements of cascading stages [PEL 98b] may not be high due mainly to the leakage current problem. To achieve the most power-efficient design, the signal conditioning system employs the half-delay-SC-integrator-based lowpass ladder filter and ΣΔ modulator, which have been described in Chapter 3. Fundamentally, if the opamps employed in those half-delay SC integrators are turned off after their integration phases, a power reduction of as much as 50% can be achieved compared with a conventional SC system that employs full-delay SC integrators, where the opamps are required to be active at all time. Besides, in a fully-differential implementation, a half-delay-SC-integrator-based system can be made parasitic-insensitive and more importantly, can be easily converted into a single-opamp-based system with a proper time-multiplexing scheme, as illustrated in Fig. 8.13.

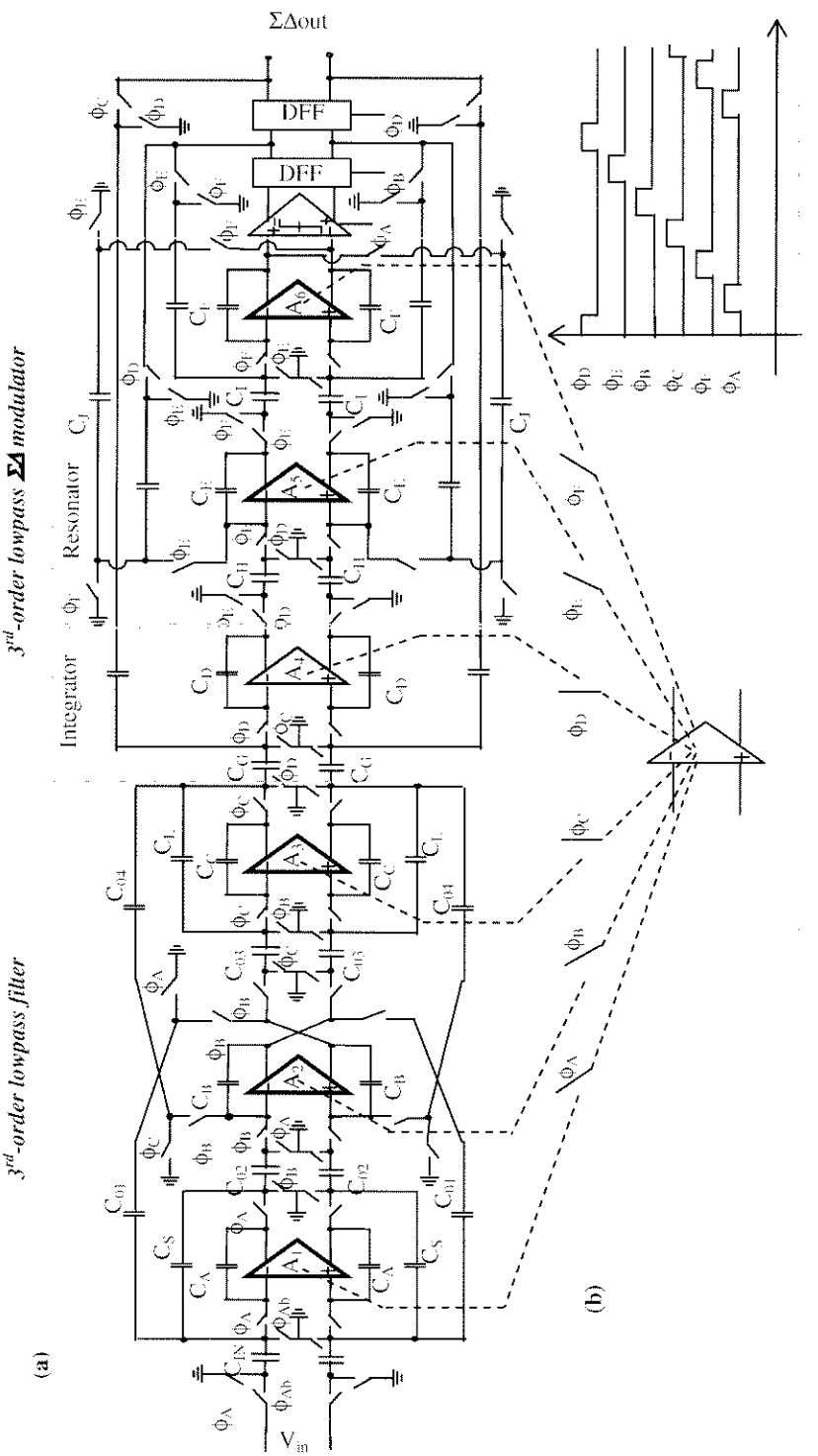


Figure 8.13 (a) Proposed Half-Delay-SC-Integrator-Based SC Signal-Conditioning System (b) Proposed Time-Multiplexing Scheme

In this proposed system, the opamps A_1 to A_6 are realizing half-delay integration function for the filter and ΣΔ modulator at non-overlapping clock phases ϕ_A to ϕ_F respectively. It can be observed that, due to the use of half-delay integrators, these opamps can be turned off after their integration phases to reduce power significantly. With this special clock phase arrangement, only one of the six opamps is required to be active at a time. As a result, with a proper time-multiplexing scheme, a single opamp can be recursively used to access all the integrator capacitors to implement the system. It also makes it possible to optimize the opamp among speed, noise and leakage requirements, and consequently, by combining with low-voltage operation, push the minimum power consumption to the sub-μW range.

Lastly, at a given total power consumption, it is interesting to point out that single-opamp-based system could still provide advantages over noise, compared with a conventional architecture that employs N opamps with each of them biased at a given current, even those N opamps are already designed to optimize for speed. This can be observed if considering the N opamps to be replaced by a single opamp that is designed to have its devices aspect ratios (W/L) and bias current N times of any of the N opamps. In this case, this single opamp could run N times faster than any one of the N opamps while its noise performance is improved by a factor of square-root N. In a best case if a cascaded system noise source is dominated by the thermal noise of the first-stage opamp (most likely to happen in a low-power and low-frequency SC systems), the total system noise can be reduced by a factor of square-root N.

8.4.1 Single-Switched-Opamp-Based Realization

As similar to the realization of the single-opamp-based ΣΔ modulator as described in section 8.4 of this chapter, a straight forward realization of the proposed system with switched-opamp technique could be achieved using a switchable opamp with six switchable output pairs [CHE 02a] as shown in Fig. 8.14. The switchable opamp consists of a PMOS input pair and six switchable output pairs, which are controlled on and off with non-overlapping clock phases ϕ_A to ϕ_F respectively. In this case, every integration capacitor ($C_{A\text{-}F}$) of the signal-conditioning system is accessed by one switchable output pair of the switchable opamp. However, since every switchable output pair is accompanied with a compensation capacitor, the slew-rate performance of the opamp are degraded severely while much more chip area is consumed. Besides, it also complicates the realization of the associated common-mode feedback circuit for differential operation.

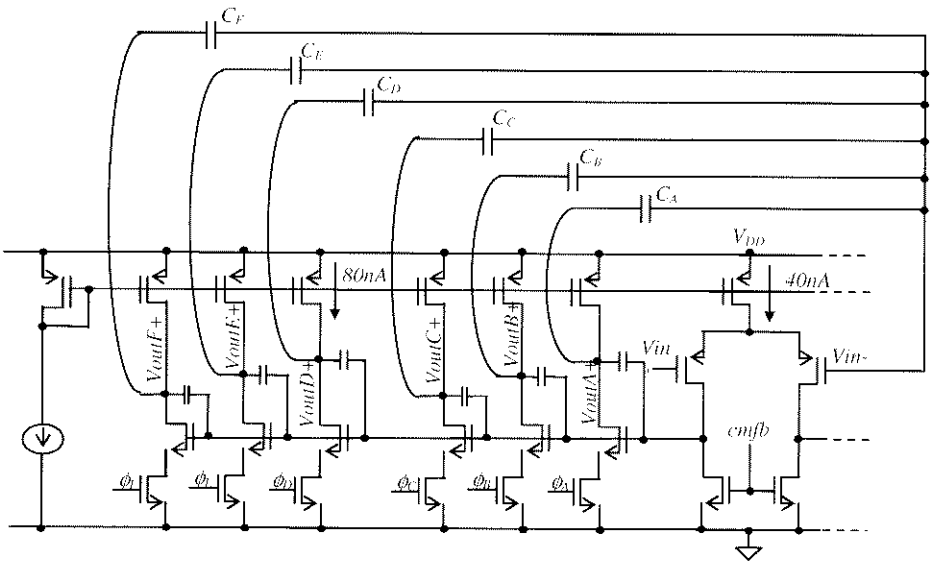


Fig. 8.14 Proposed Opamp with Six Switchable Output Pairs (Single-ended is Shown)

In the proposed system, only two pairs of switchable output stages are employed instead of using six switchable output pairs to maintain good slew-rate performance of the opamp while keeping the common-mode feedback circuits as simple as conventional switched-opamp designs. The arrangement is shown in Fig. 8.15.

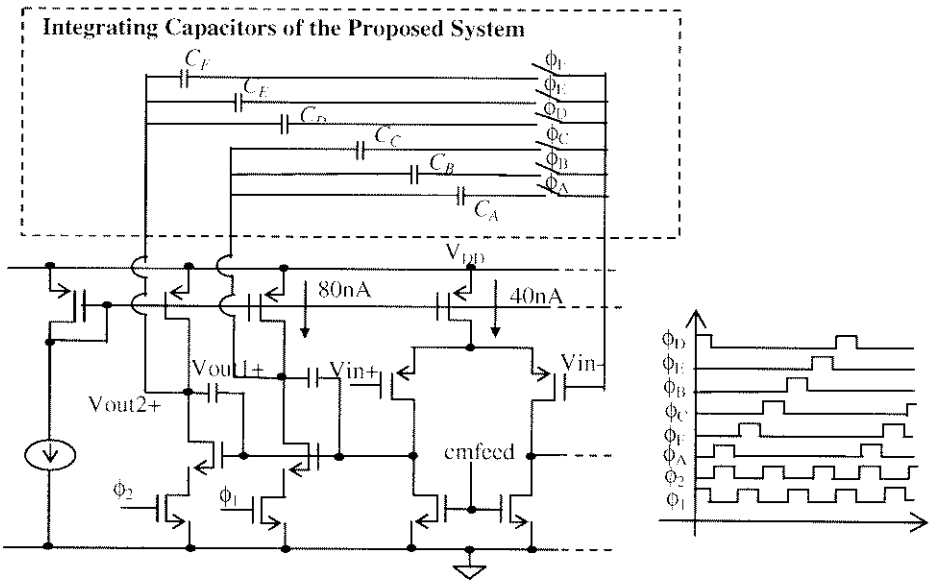


Figure 8.15 Opamp with Dual Switchable Output Pairs (Single-ended is Shown)

The opamp consists of two switchable output stages, which are turned on and off alternately with non-overlapping clock phases ϕ_1 and ϕ_2. In this arrangement, the integrator capacitors C_A, C_B, C_C, C_D, C_E and C_F are connected in feedback with the opamp only during their integration phases (ϕ_A ... ϕ_F), but kept open-connected to preserve their stored charge for their next integration events. All clock phases are generated on chip with the employment of a single master clock phase. As mentioned previously, unlike conventional single-opamp designs that suffer from stability problem during the period between non-overlapping clock phases where the change of the integrator capacitors occurs as a result of time multiplexing, the single-switched-opamp design has its opamp output shorted to V_{DD} after integration. As a result, the opamp is disconnected from the system and hence stable operation is always guaranteed. Dynamic SC level-shifters are employed to bias the common-mode voltages of the opamp input and output at ground and $V_{DD}/2$ respectively. It would be interesting to point out that, during ϕ_C, the analog output of the opamp represents the output of the lowpass filter. Besides, during ϕ_F, the output of the opamp, which represents the output signal of the last integrator of the $\Sigma\Delta$ modulator, is coupled to a latch-type comparator with a SC level shifter. The comparator is reset at ϕ_{Ab} and its output is then stored by D-flip-flops (DFF). Since the outputs of the DFFs are either V_{DD} or ground, complementary switches can be employed to feed the DFFs output back to the opamp. Cascaded DFFs are employed to realize the required feedback delay for the $\Sigma\Delta$ modulator.

Figure 8.16 shows the proposed single-switched-opamp-based design of the signal-conditioning system. To cope with the low supply voltage requirement and multi-phase operation, multi-phase switched-opamp technique is employed. Table 8.4 summarizes the value of the capacitors used.

Table 8.4 Summary of Capacitor Values

C_{IN}	2000F	C_G	175F
C_A	528F	C_K	200F
C_B	465F	C_L	200F
C_C	528F	C_M	155F
C_D	500F	C_N	135F
C_F	500F	C_S	200F
C_E	500F		
C_{01}	200F	C_{03}	200F
C_{02}	200F	C_{04}	200F

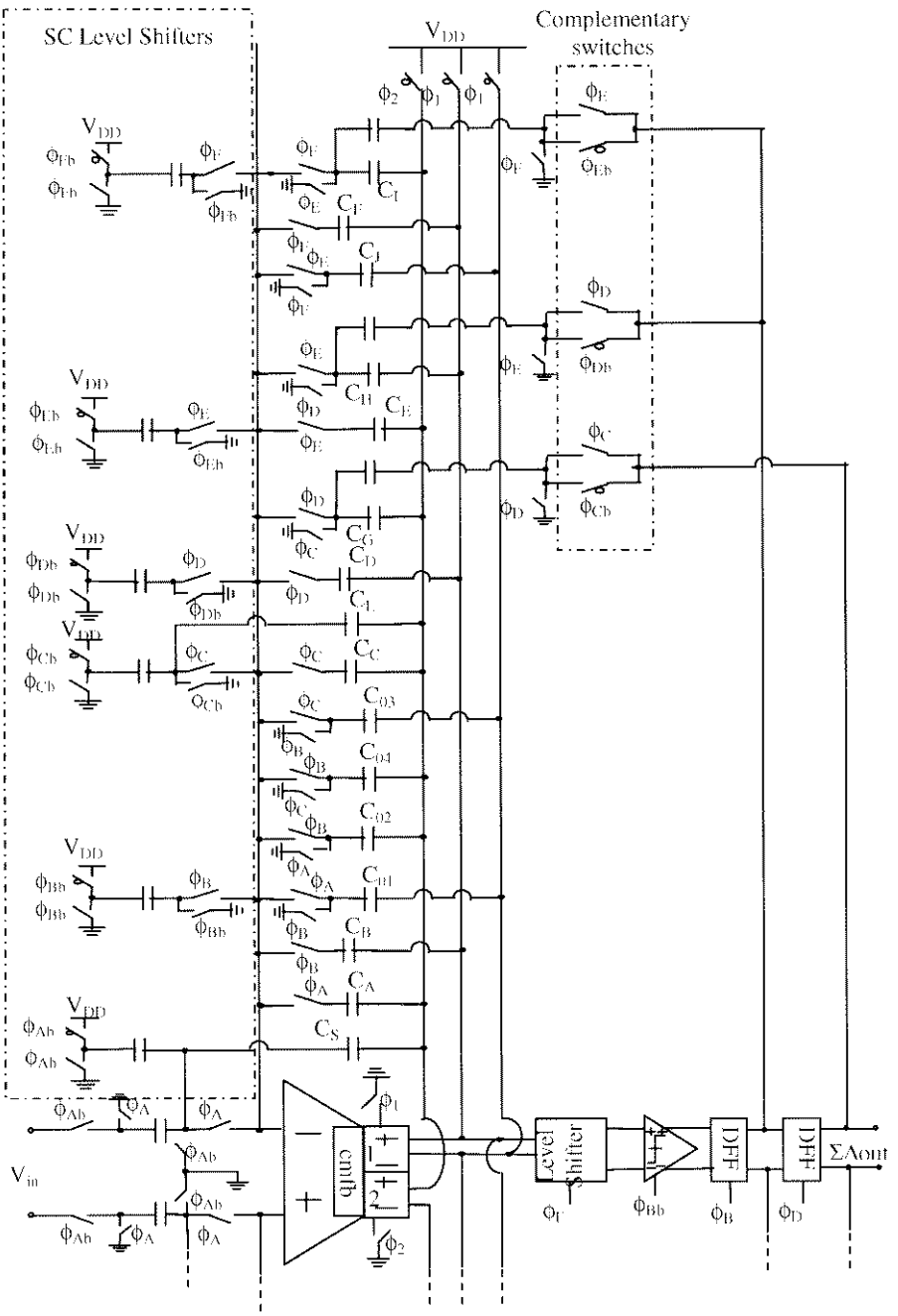


Figure 8.16 Schematic of the Proposed Single-Opamp-Based SC Signal-Conditioning System (Single-Ended Version is Shown)

8.4.2 Switchable Opamp Design

Figure 8.17 shows the schematic of the proposed switchable opamp.

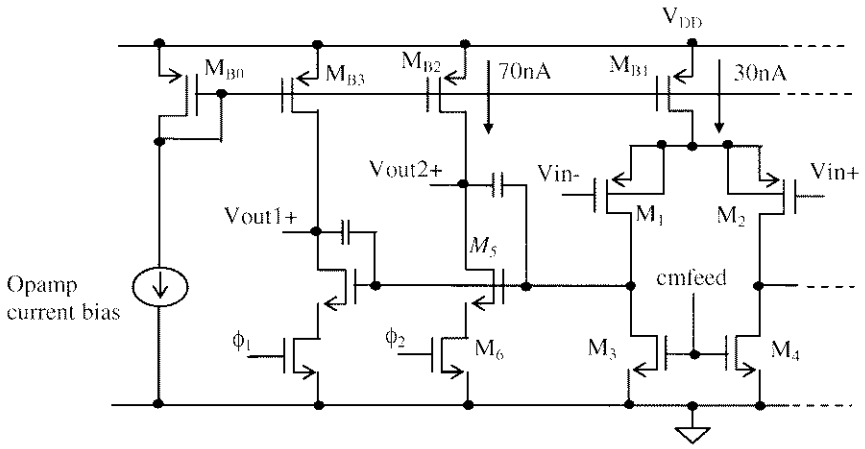


Figure 8.17 Proposed Opamp with Dual Switchable Output Pairs (Single-ended is Shown)

The design of this switchable opamp is similar as the one described in section 8.4. To reduce the Flicker's noise effect, a PMOS differential pair operates at sub-threshold region is employed as the input stage. To cope with the low supply voltage, the common-mode input voltage is set at ground. In an N-well process, it is possible to connect the bodies of the input transistors to their sources rather than connecting to the highest supply voltages to reduce the body effect, where the latter case increases the threshold voltages of the device. Only two identical switchable output pairs are controlled to turn on and off alternately by a pair of non-overlapping clock phases ϕ_1 and ϕ_2. Each of the output stages is connected to a compensation capacitor to stabilize the opamp when the output stages are turned on. Since only one output pair is turned on at a time, the differential output stage dissipates only 140 nA. Take into account the 30 nA current dissipation from the input stage and 15 nA for biasing, the opamp consumes only 185 nA.

8.4.3 Dynamic Common-Mode Feedback Circuit

Figure 8.18 shows the common-mode feedback circuit (CMFB) for the proposed opamp.

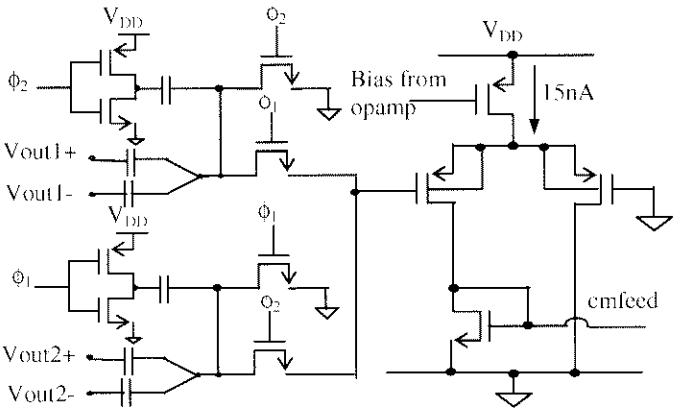


Figure 8.18 Proposed Dynamic CMFB Circuit

SC level-shifters are used to compute the common-mode output voltage of the opamp and inject the result to the error-amplifier-based CMFB [WAL 99], which is built with a differential-pair. The error signals are fed back to the opamp input stage at V_{cmfeed} to control the opamp output common-mode voltage to $V_{DD}/2$. The current consumption of the CMFB is 15nA. The performance and the size of the devices of the opamp are similar to that of the switchable opamp described in section 8.4. Table 8.5 summarizes the measured performance of the proposed switchable opamp for the single-switched-opamp signal-conditioning system.

Table 8.5 Measured Performance of Switchable Opamp

Technology	0.35-μm CMOS
Supply Voltage	0.9 V
Low Frequency Gain	75 dB
Unity Gain Bandwidth	50 kHz
Phase Margin	46°
Linear Output Swing (single-ended)	0.5 V
Power Consumption	200 nW
Loading	1 pF

8.4.4 Experimental Results of the SC Signal-Conditioning System

Figure 8.19 shows the chip photograph of the design, which is implemented in a 0.35-μm CMOS double-poly four-metal process ($VT_N = 0.6$ V, $VT_P = -0.77$ V) and occupies a chip area of about 0.2 mm^2.

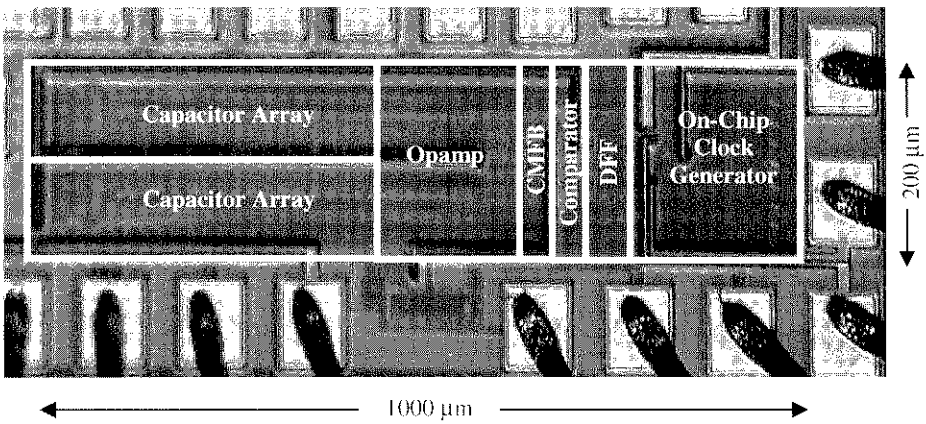


Figure 8.19 Chip Photograph of the Proposed SC Signal-Conditioning System

Figure 8.20 shows the testing setup for measuring the performance of the SC sensing system. A 50-kHz system clock is applied to the on-chip clock generator to produce a sampling frequency of 8.3 kHz to the SC signal conditioning system. Again, an off-chip single-end-to-differential converter (Fig. 8.8(b)) is employed to generate the required differential signal to the ΣΔ modulator. A simple sample-and-hold (S/H) is built on-chip to sample the output of the opamp during ϕ_C, which corresponds to the output of the filter. For measurement purposes, the NMOS switches of the S/H are driven by a 3-V on-chip inverter clocked at ϕ_C in order to access the whole opamp output swing. The held value is passed to measuring equipment through on-chip analog buffer, which is designed to operate at 3-V supply to achieve both good linearity and driving capability. Figure 8.19 shows the measured frequency response of the filter. The filter achieves a 3rd-order lowpass response with a –3-dB bandwidth of 120 Hz and a passband gain of 15 dB. A minimum stopband loss relative to passband of –25 dB is measured at frequency of 900 Hz.

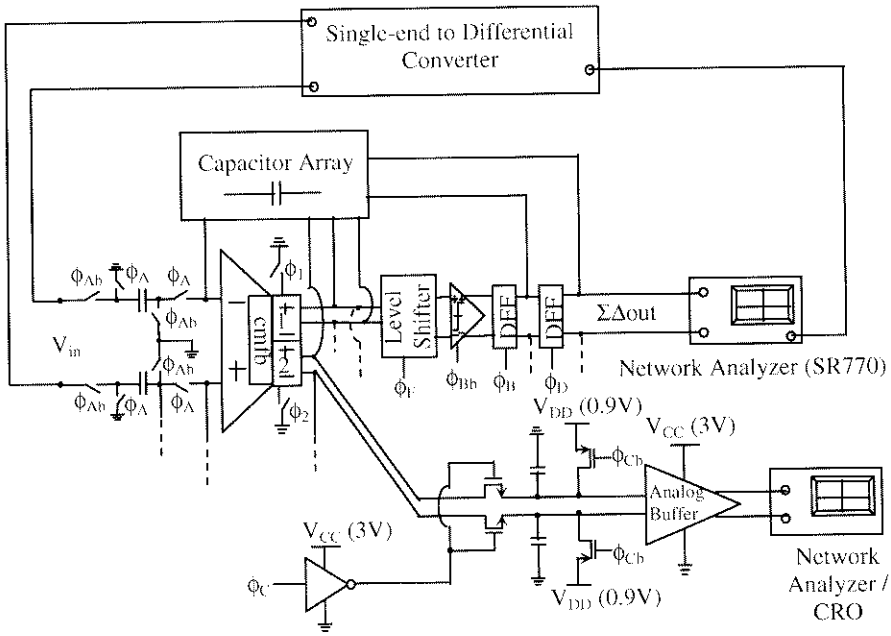


Figure 8.20 Testing Setup for Measuring the Performances of the SC Sensing System

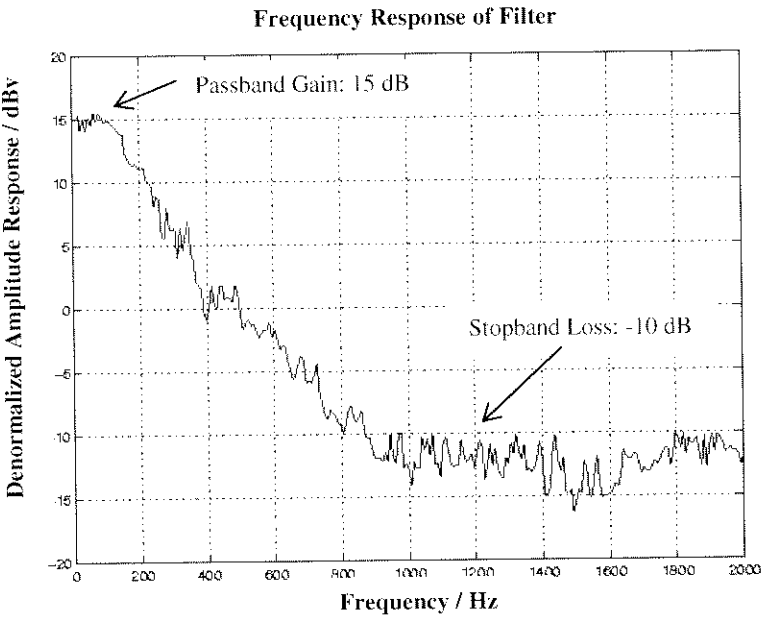


Figure 8.21 Frequency Response of the 3rd-order Ladder Filter

Figure 8.22 shows the third-harmonic distortion (THD) measurement of the filter. The third-harmonic component of an input signal (f_{in}) at 26 Hz is located at $3*f_{in}$ = 78 Hz. A 1% THD to a 0.18-V_{pp} input signal. The dynamic range of the filter, for a 1% THD, is 46 dB.

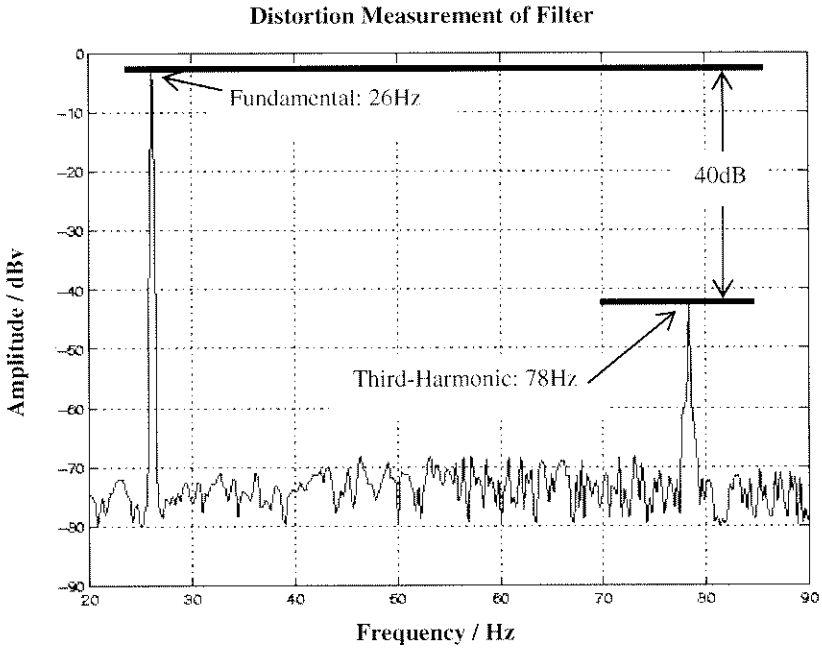


Figure 8.22 Third-Harmonic Distortion Measurement of Filter

Figure 8.23(a) shows full-span view of the output frequency spectrum of the ΣΔ modulator with a 26-Hz input signal. Figure 8.23(b) shows the zoom-in view of the interested-band of the modulator. It can be observed that a 3rd-order noise-shaping function is obtained. Figure 8.23(c) plots the in-band frequency spectrum of the ΣΔ modulator without applying input signal. As described in section 3.4, the ΣΔ modulator achieves noise-shaping extension by employing integrator to suppress the quantization noise at the DC, while using a resonator, which is placed at 65 Hz, to suppress the quantization noise at low-frequency regions. As a result, the noise-shaping region is extended to enhance the resolution without increasing the over-sampling-ratio (OSR), which in turn reduces the power consumption.

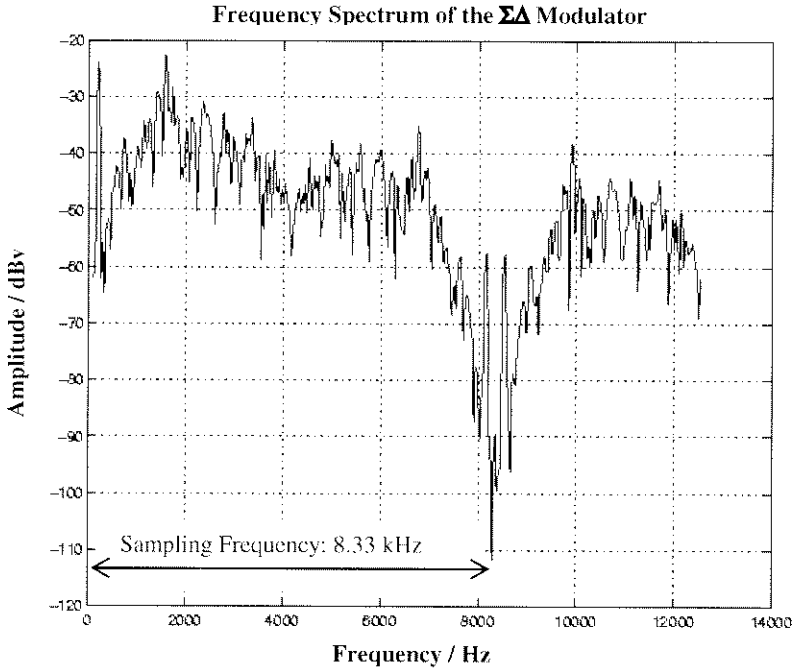


Figure 8.23 (a) Full-Span Output Frequency Spectrum of the DS Modulator

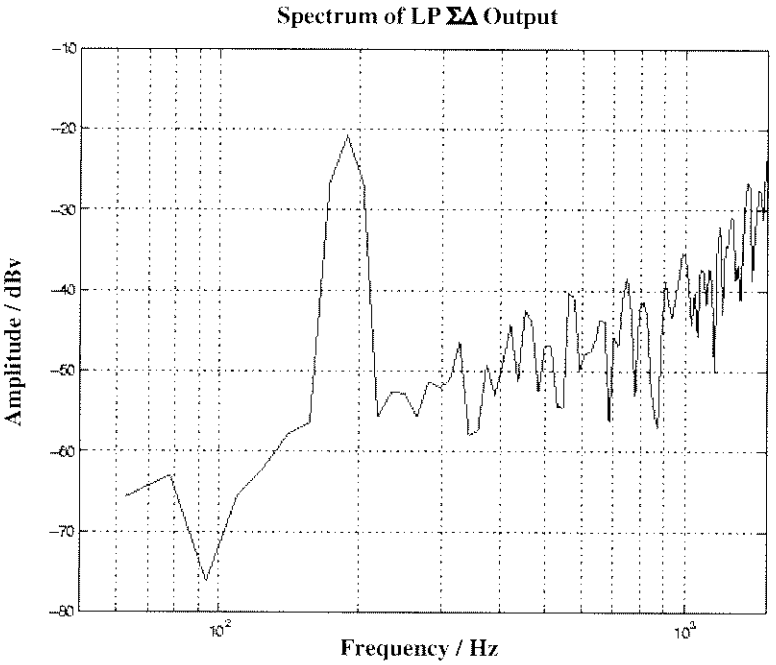


Figure 8.23 (b) Zoom-In Output Frequency Spectrum of the DS Modulator

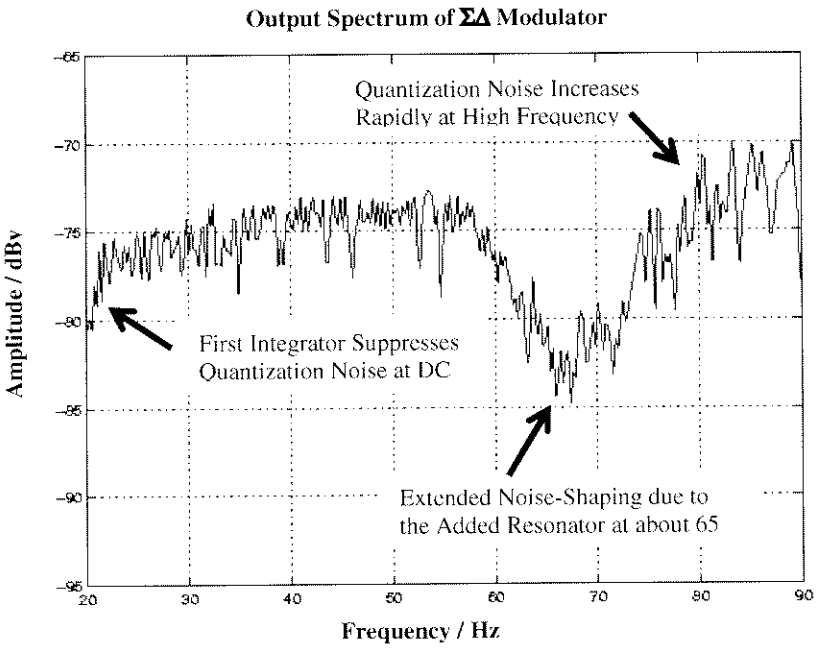


Figure 8.23 (c) Output Frequency Spectrum of the DS Modulator Without Input Signal

Figure 8.24 plots the signal-to-noise-ratio (SNR) and the signal-to-noise-plus-distortion-ratio (SNDR) as a function of the input level.

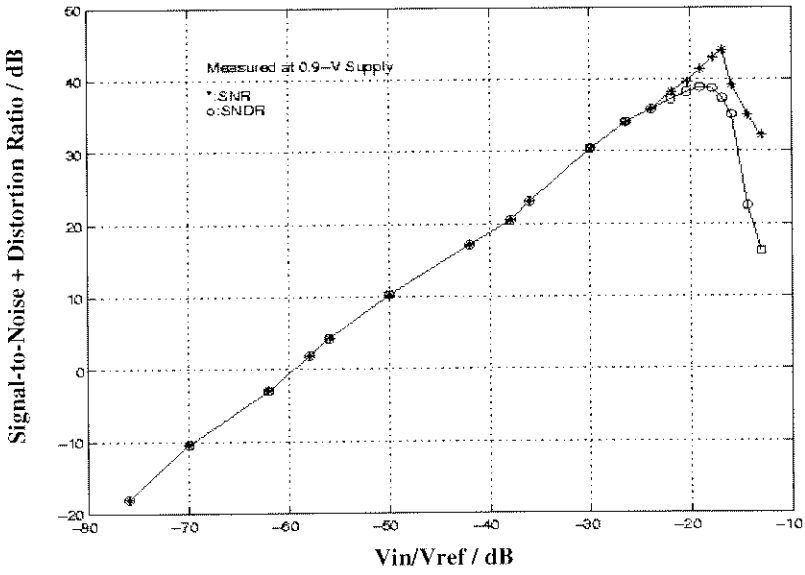


Figure 8.24 Measured SNR and SNDR vs. Input Signal Level

The SNDR is calculated using Matlab through processing the measured frequency spectrum through the FFT network analyzer (SR770). With a 0.9-V supply, the ΣΔ modulator achieves a measured peak SNDR of 39 dB with a 26-Hz input signal of –18.5 dBV at an interested signal bandwidth of 70 Hz (20 Hz to 90 Hz). The measured peak SNR is 44 dB with a 26-Hz input signal of –16.5 dBV at an interested signal bandwidth of 70 Hz. The corresponding dynamic range of the ΣΔ modulator is 45 dB. By employing single-opamp design, the whole SC signal conditioning system consumes an ultra low power of only 0.5 μW, which is reduced by more than half of that of the existing designs. Table 8.6 summarizes the overall system performance together with the state-of-the-art micro-power SC circuits.

Table 8.6 Performance Summary of the Proposed SC Signal Conditioning System and State-of-the-Art Micro-Power SC Circuits

Design	This Design	[R.CAS 90]	[A.BAS 00] *	[A.GER 00] *
Technology	0.35-μm CMOS	2-μm CMOS	0.35-μm CMOS	0.8-μm CMOS
Supply Voltage	0.9 V	+/- 1.2 V	1 V	2 V
Technique Employed	Multi-phase switched-opamp with one opamp time-multiplexed	Switched-capacitor technique with two opamps time-multiplexed	Switched-opamp without time-multiplexing of opamp	Switched-opamp technique without time-multiplexing of opamp
Type	Lowpass Filter & Lowpass ΣΔ Modulator	Bandpass Filter	Bandpass Filter	Lowpass ΣΔ Modulator
Sampling Frequency	8.33 kHz	2.048 kHz	1 kHz	8 kHz
Filter Order	Third	Sixth	Fourth	NA
Filter Dynamic Range	46 dB	55 dB	NA	NA
Passband Gain	15 dB	NA	44.5 dB	NA
Stopband Loss (relative to passband)	25 dB	NA	NA	NA
ΣΔ Modulator Order	Third	NA	NA	Third
ΣΔ Modulator Dynamic Range	45 dB	NA	NA	55 dB
ΣΔ Modulator Peak SNR / SNDR	44 dB / 39 dB	NA	NA	NA
Chip Area	0.2 mm^2	1.4 mm^2	NA	NA
Power Consumption	Analog: 0.2 μW Digital: 0.3 μW	Analog: 1 μW Digital: NA	Analog: 1.2 μW Digital: NA	Analog: 2 μW Digital: NA
* Simulation results				

8.5 Conclusion

Biomedical ICs are usually provided with very minimal power and chip-area budgets for battery and implantability concerns. A single-opamp-based system is demonstrated to be a good candidate to cope with these tight budgets. By employing a switched-opamp technique and one switchable opamp, sub-μW operation of a ΣΔ modulator and a SC signal conditioning system are demonstrated at a single 0.9-V supply. Robust operation is also observed for both designs at supply voltages from 0.8 V to 1.2 V.

Chapter 9

CONCLUSION

In this book, the limitations and design issues of switched-opamp circuits have been addressed. Efforts have been put on the development of novel system architectures and circuit design techniques for switched-opamp circuits. Through theoretical analysis and circuits implementations, the limitations of the original switched-opamp technique, which requires the opamp to be turned off after integration, are resolved successfully with the proposed multi-phase switched-opamp technique, which enables SC systems to have opamps active at all time. As a result, it significantly improves the compatibility of switched-opamp technique on conventional SC architectures as demonstrated with a circuit prototype of a 1-V SC Pseudo-2-Path Filter.

Detailed theoretical analyses of both of the original switched-opamp technique and multi-phase switched-opamp technique have also shown that the employment of the multi-phase switched-opamp technique could maintain a low sensitivity of SC circuits to a finite gain of the opamp. In order to improve the operation speed and power efficiency of SC systems at low-voltage operation, new system and circuit designs are developed. On the system level, the study of the speed limitations of the conventional double-sampled SC filter architecture suggests decoupling the active elements for independent settling. The idea is further illustrated through the realization of a generic fast-settling double-sampling SC biquadratic filter for a high-speed switched-opamp bandpass $\Sigma\Delta$ modulator. The chip prototype achieves a measured sampling frequency reached up to 50 MHz, which is more than ten-times improvement over prior switched-opamp designs and comparable to the performance of the state-of-the-art SC circuits that operate at much higher supply voltages. Accompanied with a low-voltage finite-gain-compensation technique, low-voltage low-power and high-speed operation of switched-opamp circuits is successfully demonstrated.

In addition, a family of half-delay-SC-integrator-based SC filters and $\Sigma\Delta$ modulator has been proposed. Implemented with the proposed switched-opamp techniques, these systems achieve up to a 50 % power reduction while maintaining low sensitivity to finite opamp gain effects as for the conventional switched-capacitor realization.

The proposed noise-shaping extension technique is shown to maximize the achievable signal-to-noise-ratio of a 3rd-order lowpass ΣΔ modulator by at least 16 dB without dissipating extra power. Further development of the proposed half-delay-SC-integrator-based systems leads to the realization of a single-opamp-based system for ultra-low-power applications. By employing the switched-opamp technique and one switchable opamp, sub-μW operation of a ΣΔ modulator and a SC signal conditioning system are demonstrated at a single 0.9-V supply. Robust operation is also observed for both designs at supply voltages from 0.8 V to 1.2 V.

On the circuit level, the study of different switching methodologies suggests keeping the input stage of a two-stage opamp active all the time while switching only the output stages. For maximum speed operation, the output stages may take turns sharing one bias current source that is always on to reduce the turn-on time. The successful integration of a 1-V low-power switched-opamp IF circuitry for Bluetooth receivers demonstrates, with the availability of low-voltage low-power CMOS front-end circuits, the feasibility to achieve single 1-V low-power CMOS wireless transceivers.

Altogether, the developed low-voltage techniques and the proposed low-power systems make it possible to significantly extend the battery life for portable equipment and, in a broader sense, to further advance the progress on single-chip integration of mixed-signal systems with sub-micron CMOS technologies.

Appendix A

PROCEDURES OF PERFORMING TIME-DOMAIN ANALYSIS OF SWITCHED-CAPACITOR CIRCUITS

The procedures of performing time-domain analysis of switched-capacitor circuits are extracted from reference [KI 95] and summarized here.

Conditions:
Opamp non-idealities such as finite-opamp again (A_o) and offset voltage (V_{os}) can be included when performing time-domain analysis of switched-capacitor circuits. On the other hand, opamp bandwidth and switch-on-resistance are assumed perfect.

Methodology:
Apply Kirchhoff Charge Law (KQL), which stated that:

> ***In a switched–capacitor circuit, the sum of all charges leaving any non-source node at any instance of charge transfer equals zero.***

Steps:
1) For all capacitors, the left plate is designated to be positive, while the right plate negative as illustrated in Fig. A1.
2) Charge transfer occurs at the instants of the clock, which happens at t=nT, i.e. phase1 (ϕ_1), and t=(n-1/2)T, i.e. phase 2 (ϕ_2), where ϕ_1 and ϕ_2 are non-overlapping clock phases.
3) Divide capacitors into two groups:
   -One group is to the right of the inverting node (V-) at the opamp (the right-hand group (RHG)), while the other is to the left (the left-hand group (LHG)).
4) Construct a table to keep track of the change of the branch voltages of the capacitors.

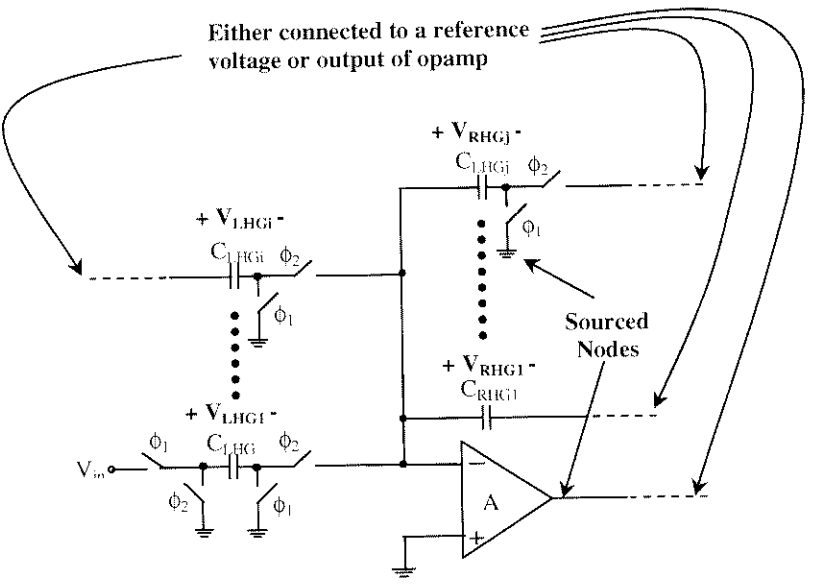


Figure A1 Application of KQL in SC Circuits

Setting Up Equations:

1) By KQL, the change in the charge in the RHG must equal to the LHG

i.e. $\Delta Q_{LHG} = \Delta Q_{RHG}$

$$\Rightarrow \sum_{i=1}^{N} \Delta Q_{LHGi} = \sum_{j=1}^{M} \Delta Q_{RHGj}$$

Or equivalently,

$$\Rightarrow \sum_{i=1}^{N} C_{LHGi}\left[V_{LHGi}\left[(n+1)T\right] - V_{LHGi}(nT)\right] = \sum_{j=1}^{M} C_{RHGi}\left[V_{RHGj}\left[(n+1)T\right] - V_{RHGj}(nT\right.$$

2) Each opamp (each inverting node) corresponds to one of this equations.

Caution:

Additional equations are needed for parasitic sensitive circuits.

Appendix B

The Effects of the Finite Opamp DC Gain on Conventional Inverting Switched-Capacitor Integrator

Figure B1 shows the schematic of a conventional inverting switched-capacitor integrator. To analyze the finite-opamp-gain effects of this integrator, the opamp is assumed to be ideal except with a finite DC gain of A_o, while all capacitors and switches are considered perfect. Table B1 is constructed to perform the time-domain analysis of the inverting SC integrator with output V_{out1}.

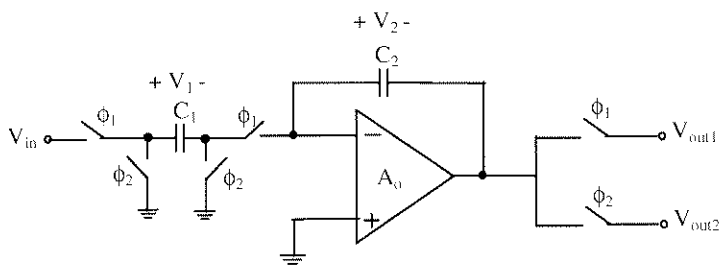


Figure B1 Parasitic-Insensitive Inverting SC Integrator

Table B1 Timing Diagram Showing the Charge Transferring that Occurs at All Capacitors

$\phi_2 = 1, \left[\left(n - \frac{1}{2}\right)T, nT\right]$	$\phi_1 = 1, \left[nT, \left(n + \frac{1}{2}\right)T\right]$	Cap
$V_1\left[\left(n - \frac{1}{2}\right)T\right] = 0$	$V_1(nT) = V_{IN}(nT) + \frac{V_{out1}(nT)}{A_o}$	C1
$V_2\left[\left(n - \frac{1}{2}\right)T\right] = -\frac{V_{out1}\left[\left(n - \frac{1}{2}\right)T\right]}{A_o} - V_{out1}\left[\left(n - \frac{1}{2}\right)T\right]$	$V_2(nT) = -\frac{V_{out1}(nT)}{A_o} - V_{out1}(nT)$	C2

Note that: $V_{out1}(nT) = V_{out2}\left[\left(n + \frac{1}{2}\right)T\right]$

By Kirchhoff Charge Law, during $\phi_2 \rightarrow \phi_1$ transition, i.e. from time (n-1/2) to (n), the change in charge of capacitor C_1 (ΔQ_1) is equal to that of capacitor C_2 (ΔQ_2).

$$i.e.\ \Delta Q1 = \Delta Q2$$

$$\Rightarrow C_1\left[V_{IN}(nT) + \frac{V_{out1}(nT)}{A_o}\right]$$

$$= C_2\left[-\frac{V_{out1}(nT)}{A_o} - V_{out1}(nT) + \frac{V_{out1}[(n-1)T]}{A_o} + V_{out1}[(n-1)T]\right]$$

$$\Rightarrow C_1[V_{IN}(nT)] = -\left[\frac{C_1}{A_o} + \frac{C_2}{A_o} + C_2\right][V_{out1}(nT)] + \left[\frac{C_2}{A_o} + C_2\right][V_{out1}[(n-1)T]]$$

By z-transformation, the z-domain transfer function of the conventional inverting SC integrator with output taken at V_{out1} during ϕ_1 is given by:

$$H_1(z) = \frac{V_{out1}(z)}{V_{IN}(z)} = \frac{-C_1}{\left[\frac{C_1 + C_2}{A_o} + C_2\right] - \left[\frac{C_2}{A_o} + C_2\right]z^{-1}}$$

The ideal transfer function of the inverting SC integrator with infinite opamp gain is given by:

$$H_{Ideal}(z) = \frac{V_{out1}(z)}{V_{IN}(z)} = \frac{-C_1}{C_2\left(1 - z^{-1}\right)}$$

It can be observed that the gain of the integrator has been reduced from C_1/C_2 to a smaller value due to the finite opamp gain. Also, the pole has now a smaller positive value. To investigate the finite-opamp-gain effects to the frequency response of the integrator, the transfer function of the integrator is written in term of the ideal transfer function [GRE 86]:

$$\frac{H_{Ideal}(z)}{H_1(z)} = \frac{\left[\frac{C_1 + C_2}{A_o} + C_2\right] - \left[\frac{C_2}{A_o} + C_2\right]z^{-1}}{C_2\left(1 - z^{-1}\right)}$$

$$= \frac{\left[1+\left(\frac{1+C_1/C_2}{A_o}\right)\right]-\left[1+\frac{1}{A_o}\right]z^{-1}}{1-z^{-1}}$$

$$= \frac{\left[1+\left(\frac{1+C_1/2C_2}{A_o}\right)+\frac{C_1/2C_2}{A_o}\right]-\left[1+\left(\frac{1+C_1/2C_2}{A_o}\right)\right]z^{-1}+\left(\frac{C_1/2C_2}{A_o}\right)z^{-1}}{1-z^{-1}}$$

$$= 1+\left(\frac{1+C_1/2C_2}{A_o}\right)+\left(\frac{C_1/2C_2}{A_o}\right)\left(\frac{1+z^{-1}}{1-z^{-1}}\right)$$

Substituting $z = e^{j\omega T}$,

$$\frac{H_{Ideal}\left(e^{j\omega T}\right)}{H_1\left(e^{j\omega T}\right)} = 1+\left(\frac{1+C_1/2C_2}{A_o}\right)+\left(\frac{C_1/2C_2}{A_o}\right)\left(\frac{e^{\frac{j\omega T}{2}}+e^{\frac{-j\omega T}{2}}}{e^{\frac{j\omega T}{2}}-e^{\frac{-j\omega T}{2}}}\right)$$

$$= 1+\left(\frac{1+C_1/2C_2}{A_o}\right)-j\left(\frac{C_1/2C_2}{A_o\tan\left(\frac{\omega T}{2}\right)}\right)$$

$$\Rightarrow H_1\left(e^{j\omega T}\right) = \frac{H_{Ideal}\left(e^{j\omega T}\right)}{1+\left(\frac{1+C_1/2C_2}{A_o}\right)-j\left(\frac{C_1/2C_2}{A_o\tan\left(\frac{\omega T}{2}\right)}\right)}$$

$$= \frac{H_{Ideal}\left(e^{j\omega T}\right)}{1-m(\omega)-j\theta(\omega)} = F(\omega)H_{Ideal}\left(e^{j\omega T}\right)$$

where

$$m(\omega)=-\frac{1}{A_o}\left(1+\frac{C_1}{2C_2}\right)$$

$$\theta(\omega)=\frac{C_1/C_2}{2A_o\tan\left(\frac{\omega T}{2}\right)}\approx\frac{C_1/C_2}{A_o\omega T}$$

The error factor F(ω) introduced by the finite-opamp-gain effects into the frequency response of the inverting SC integrator can be written in the polar form:

$$F(\omega)=|F(\omega)|e^{j\angle F(\omega)}$$

where

$$|F(\omega)|^2=\frac{1}{[1-m(\omega)]^2+[\theta(\omega)]^2}\approx\left[\frac{1}{1-m(\omega)}\right]^2\approx[1+m(\omega)]^2$$

and

$$\angle F(\omega)=-\tan^{-1}\left[\frac{-\theta(\omega)}{1-m(\omega)}\right]\approx\tan^{-1}\theta(\omega)\approx\theta(\omega)$$

$$\Rightarrow F(\omega)\approx[1+m(\omega)]e^{j\theta(\omega)}=\left[1-\frac{1}{A_o}\left(1+\frac{C_1}{2C_2}\right)\right]e^{j\left(\frac{C_1/C_2}{A_o\omega T}\right)}$$

Thus, m(ω) represents the relative magnitude error, while θ(ω) the phase error in radians caused by the finite-opamp-gain effects. Considering when the integrator is operating at its unity-gain frequency ω_i, at which

$$H_{Ideal}\left(e^{j\omega_i T}\right)=1$$

$$\Rightarrow\frac{C_1}{C_2}=2\sin\left(\frac{\omega_i T}{2}\right)$$

$$\Rightarrow m(\omega_i)=-\frac{1}{A_o}\left[1+\sin\left(\frac{\omega_i T}{2}\right)\right]$$

For $\omega_i << \omega_s$, where ω_s is the sampling frequency of the circuit,

$$\Rightarrow \sin\left(\frac{\omega_i T}{2}\right) \approx 0$$

$$\Rightarrow m(\omega_i) \approx -\frac{1}{A_o}$$

and

$$\theta(\omega_i) = \frac{1}{A_o}\cos\left(\frac{\omega_i T}{2}\right) \approx \frac{1}{A_o}$$

Implications: The magnitude error $m(\omega)$ can be regarded as the deviation of the designed gain of the integrator C_1/C_2 from its nominal value by a relative error of $1/A_o$, while the finite opamp gain also introduces a relative phase error of $1/A_o$.

Lastly, the z-transfer function of the conventional inverting SC integrator with output taken at V_{out2} during ϕ_2 is given by:

$$H_2(z) = \frac{V_{out2}(z)}{V_{IN}(z)} = \frac{-C_1 z^{-1/2}}{\left[\frac{C_1 + C_2}{A_o} + C_2\right] - \left[\frac{C_2}{A_o} + C_2\right] z^{-1}} = H_1(z) z^{-1/2}$$

The transfer function is different from the one with output being taken at V_{out1} by a half delay $z^{-1/2}$. The ideal transfer function of the inverting SC integrator with infinite opamp gain is given by:

$$H_{Ideal}(z) = \frac{V_{out2}(z)}{V_{IN}(z)} = \frac{-C_1 z^{-1/2}}{C_2\left(1 - z^{-1}\right)}$$

The half-delay $z^{-1/2}$ is cancelled when writing the actual transfer function $H_2(z)$ in term of its ideal equation. As a result, the sensitivity of the inverting SC integrator is the same no matter at which clock phase its output is taken.

Appendix C

Design Procedures of Switched-Capacitor Biquadratic Filter

Brief Review

An s-domain (continuous-time domain) second-order transfer function with complex poles as shown in Equation C1:

$$H(s)=\frac{N(s)}{D(s)}=\frac{N(s)}{1+\frac{1}{Q}\frac{s}{\omega_o}+\frac{s^2}{\omega_o^2}} \qquad \text{(Eq. C1)}$$

where ω_o and Q are respectively the interested pole frequency (in rad/sec) and the quality factor of the pole. Specifically, $f_o=\omega_o/2\pi$ and Q specify the center frequency and the quality factor of a continuous-time bandpass filter where its bandwidth is defined as f_o/Q. There exist many kinds of z-transformations such as LDI transformation, bilinear transformation, forward/backward Euler transformations and so on [GRE 86]. Among them, the bilinear transformation provides more robust performance over most of the frequency range while the rest of the z-transformations would require a sampling frequency much higher than the interested frequency range to preserve the accuracy and robustness.

Bilinear Transformation

When applying the bilinear transformation, the s-domain transfer function is converted into its z-domain counterpart through Equation C2:

$$s=2f_s\frac{1-z^{-1}}{1+z^{-1}} \qquad \text{(Eq. C2)}$$

where f_s=1/T is the sampling frequency employed in the discrete-time domain. Besides, the pole of the s-domain transfer function is pre-wrapped into the z-domain through Equation C3:

$$\Omega_o = 2 f_s \tan\left(\frac{\omega_o}{2 f_s}\right) = 2 f_s \tan\left(\frac{\pi f_o}{f_s}\right) \qquad \text{(Eq. C3)}$$

Consequently, the s-domain transfer function can be transformed in the z-domain (discrete-time domain) counterpart as given by Equation C4:

$$H(z) = \frac{N^*(z)}{D^*(z)} = \frac{N^*(z)}{\left(X_o^2 + \frac{X_o}{Q} + 1\right) - \left(2X_o^2 - 2\right)z^{-1} + \left(X_o^2 - \frac{X_o}{Q} + 1\right)z^{-2}} \qquad \text{(Eq. C4)}$$

where N*(z) and D*(z) represent the pre-wrapped zeros and poles in the z-domain and X_o=2f_s/Ω_o. For $\Omega_o << f_s$, α and β can be defined as:

$$\alpha = \frac{4}{X_o^2 + \frac{X_o}{Q} + 1} \approx \left(\frac{\Omega_o}{f_s}\right)^2$$

$$\beta = \left(\frac{X_o}{2Q}\right)\left(\frac{4}{X_o^2 + \frac{X_o}{Q} + 1}\right) \approx \frac{\Omega_o}{Q f_s}$$

The corresponding z-domain transfer function can be expressed as given in Equation C5:

$$H(z) = \frac{N^*(z)}{D^*(z)} = \frac{N^*(z)}{1 - (2 - \alpha - \beta)z^{-1} + (1 - \beta)z^{-2}} \qquad \text{(Eq. C5)}$$

where (1-β) represents the attenuation factor while (α+β) sets the pole frequency of the transfer function. There exist many generic switched-capacitor biquadratic architectures from which Equation C5 can be realized by setting appropriate capacitor ratios.

Appendix D

DESIGN PROCEDURES OF SWITCHED-CAPACITOR LADDER FILTER

Quick design procedures [GRE 86] of a fifth-order switched-capacitor lowpass ladder filter can be obtained by emulating the passive components of a fifth-order LCR filter prototype [GRE 86] with switched-capacitor circuits. Figure D1 shows a 5th-order Chebyshev LCR filter prototype, which consists of inductors, capacitors and termination resistors.

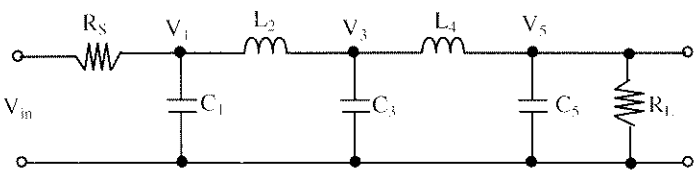


Figure D1 A 5th-Order LCR Filter Prototype Circuit

Given a required passband cut-off frequency (f_{PB}), a minimum attenuation (A_{SL}) and a stopband frequency (f_{SB}), the values of the inductors and capacitors can be obtained from most of the filter design handbooks [NIE 89]. For designing a switched-capacitor filter, the termination resistors (R_S and R_L) are normalized to 1Ω. Since a switched-capacitor lowpass filter usually employs a sampling frequency much higher than the interested passband frequency, hence LDI-transformation [GRE 86] can be used to accurately transform the continuous-time LCR filter prototype into its corresponding switched-capacitor ladder filter, which is shown in Fig. D2. The resultant filter architecture is the simplest in realization compared with employing other transformations.

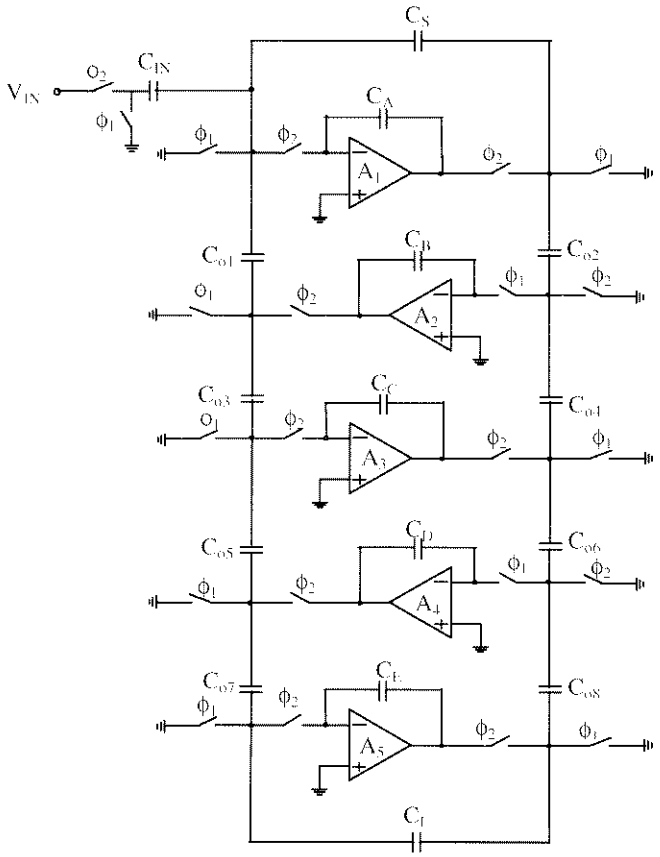


Figure D2 LDI-Transformed Switched-Capacitor Lowpass Ladder Filter

It is important to emphasize that the passband gain and the passband limit of a LCR filter prototype is pre-set to be unity and 1 rad/sec respectively. In order to obtain the designed filter characteristics, the designed passband cut-off frequency (f_{PB}) is pre-wrapped via the LDI-transformation with Equation D1:

$$\Omega_o = 2 f_s \sin\left(\frac{\pi f_{PB}}{2 f_s}\right) \qquad \text{(Eq. D1)}$$

where f_s stands for the sampling frequency used in the switched-capacitor filter. By taking C_o=1, Z_o=1/ω_a and L_o=1/ω_a^2, the denormalized LCR filter prototype parameters can be obtained by multiplying the values capacitors, inductors and resistors with C_o, L_o and Z_o respectively as shown in Table D1:

Table D1 Summary of Denomarlized Component Values of LCR Filter Prototype

$$C_1^{FT} = C_1 \qquad L_2^{FT} = L_2 \cdot L_o \qquad R_S^{FT} = R_S \cdot Z_o$$
$$C_2^{FT} = C_2 \qquad L_4^{FT} = L_4 \cdot L_o \qquad R_L^{FT} = R_L \cdot Z_o$$
$$C_3^{FT} = C_3$$

The value of the capacitors of the corresponding switched-capacitor ladder filter are related to the denomarlized component values of the LCR filter prototype as shown in Table D2:

Table D2 Summary of Value of Capacitors of the Switched-Capacitor Ladder Filter

$$C_A = C_1^{FT} \qquad C_S = \frac{T}{R_S^{FT}}$$
$$C_B = L_2^{FT} \qquad C_L = \frac{T}{R_L^{FT}}$$
$$C_C = C_3^{FT}$$
$$C_D = L_4^{FT}$$
$$C_E = C_5^{FT}$$
$$C_{01} = C_{02} = C_{03} = C_{04} = C_{05} = C_{06} = C_{07} = C_{08} = T$$

The capacitors C_{01}, C_{02}, C_{03}, C_{04}, C_{05}, C_{06}, C_{07} and C_{08} are arbitrarily chosen to be equal to the sampling period of the switched-capacitor filter. These values will be readjusted in any case by the scaling processes of switched-capacitor filters such as the dynamic range optimization and the capacitance spread reduction [GRE 86].

These design procedures can be extended to design other switched-capacitor ladder filters with different order and frequency response [GRE 86].

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